TELEDYNE DALSA

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X64 Xcelera-CL+ PX8™

User's Manual

Edition 1.00

Part number OC-X8CM-PUSR0

NOTICE

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Overview

Product Part Numbers

X64 Xcelera-CL+ PX8 Board

Item	Product Number
X64 Xcelera-CL+ PX8 Full with 256 MB of memory X64 Xcelera-CL+ PX8 Dual Base with 256 MB of memory	OR-X8C0-XPF00 OR-X8C0-XPD00
For OEM clients, this manual in printed form, is available on request	OC-X8CM-PUSR0

Table 1: X64 Xcelera-CL+ PX8 Board Product Numbers

X64 Xcelera-CL+ PX8 Software

Item	Product Number
Sapera LT version 6.30 or later (required but sold separately) 1. Sapera LT: Provides everything you will need to build your imaging application. Sapera 7.10 required for full feature support. 2. Current Sapera compliant board hardware drivers 3. Board and Sapera documentation (compiled HTML help, and Adobe Acrobat® (PDF) formats)	OC-SL00-0000000
(optional) Sapera Processing Imaging Development Library includes over 600 optimized image-processing routines.	Contact Sales at Teledyne DALSA

Table 2: X64 Xcelera-CL+ PX8 Software Numbers

X64 Xcelera-CL+ PX8 Cables & Accessories

Item	Product Number
CMD cable assembly (I/O 15 pin Micro D connector with 6 ft. blunt end cable) This cable assembly connects to J1. (see "J1 CMD15 Female External Signals Connector Descriptions" on page 103)	OR-X8CC-IO15P
(optional) X64 Xcelera-CL+ PX8 can be shipped with an External Signals Connector Bracket Assembly, either with a **DB37 or DB25** connector (see the two product numbers below). Either cable, if required, is specified at the time of order. Note: clients requiring a limited number of I/Os, can also use the CMD15 connector that is on the main bracket.	
DB37 assembly See "External Signals Connector Bracket Assembly (Type 1)" on page 109. This cable assembly connects to J4.	OR-X4CC-IOCAB
DB25 assembly See "External Signals Connector Bracket Assembly (Type 2)" on page 111. Provides direct compatibility with external cables made for products such as the X64-CL iPro. This cable assembly connects to J4.	OR-X4CC-0TIO2
(optional) Cable assembly to connect to J11 (RS-422 Shaft Encoder Inputs)	Contact Sales at Teledyne DALSA
(optional) Power interface cable required when supplying power to cameras	OR-COMC-POW03
(optional) Power Over Camera Link (PoCL) Video Input Cable 2 meter HDR to MDR 2 meter HDR to HDR	 OR-COMC-POCLD2 OR-COMC-POCLDH

Table 3: X64 Xcelera-CL+ PX8 Cables & Accessories

About the X64 Xcelera-CL+ PX8 Frame Grabber

Series Key Features

- Available either as a Full or Dual Base Camera Link board
- Uses a PCIe x8 slot to maximize transfers to host computer buffers
- Acquire from Monochrome, Bayer Filter or RGB Cameras, both area scan and linescan
- Supports multiple tap formats and multiple tap scan directions, in multiple pixels depths
- Pixel clock range from 20 to 85 MHz
- On board hardware Flat Field Correction
- Output lookup tables
- Vertical and Horizontal Flip supported on board
- External Input Triggers and Shaft Encoder inputs (either opto-coupled or TTL/RS422), along with Strobe outputs
- Supports a number of acquisition events in compliance with "Trigger to Image Reliability"
- RoHS compliant
- Supports Power Over Camera Link (PoCL)

See "Technical Specifications" on page 89 for detailed information.

User Programmable Configurations

Use the X64 Xcelera-CL+ PX8 firmware loader function in the Teledyne DALSA Device manager utility to select firmware for one of the supported modes. Firmware selection is made either during driver installation or manually later on (see "Firmware Update: Manual Mode" on page 17).

Full board: Firmware choices are:

- **One Full Camera Link Input with Flat Field Correction** (*installation default selection*):
  Support for 1 Base, 1 Medium or 1 Full Camera Link camera. Flat Field Correction (FFC) includes Fixed Pattern Noise (FPN), Pixel Replacement, Photo Response Non Uniformity (PRNU), and Shading Correction.
- **One Full Camera Link Input with Bayer Filter Decoding**:
  Support for one Base, one Medium or one Full Camera Link camera with Hardware Bayer CFA (Color Filter Array) Decoder. Flat Field Correction is not available in this configuration.
- **One Camera Link Input with 10 Taps @ 8 bits with Flat Field Correction:**
  Supports cameras such as the Basler A504. See "Supporting Non-Standard Camera Link Cameras" on page 72 for details.
- **One Camera Link Input with 10 Taps @ 8-bits and 8 Taps @ 10 bits with Flat Field Correction:**
  Supports camera such as the Basler A406. See "Supporting Non-Standard Camera Link Cameras" on page 72 for details.

Dual board: Firmware choices are:

- **Two independent Base Camera Link Input with Flat Field Correction** (*installation default selection*)
  Support for one or two Base Camera Link cameras. Flat Field Correction (FFC) includes Fixed Pattern Noise (FPN), Pixel Replacement, Photo Response Non Uniformity (PRNU), and Shading Correction.
- **Two independent Base Camera Link Input with Bayer Filter Decoding:**
  Support for one or two Base Camera Link cameras with Hardware Bayer CFA (Color Filter Array) Decoder. Flat Field Correction is not available in this configuration.
- **One Medium Camera Link Input with Flat field correction:**
  Support for one Base or one Medium Camera Link camera. Flat Field Correction (FFC) includes Fixed Pattern Noise (FPN), Pixel Replacement, Photo Response Non Uniformity (PRNU), and Shading Correction.
- **One Medium Camera Link Input with Bayer Filter Decoding**:
  Support for one Base or one Medium Camera Link camera with Hardware Bayer CFA (Color Filter Array) Decoder. Flat Field Correction is not available in this configuration.

ACUPlus: Acquisition Control Unit

ACUPlus consists of a grab controller, one pixel packer, and one time base generator. ACUPlus delivers a flexible acquisition front end and supports pixel clock rates of up to 85MHz.

ACUPlus acquires variable frame sizes up to 256KB per horizontal line and up to 16 million lines per frame. ACUPlus can also capture an infinite number of lines from a line scan camera without losing a single line of data.

ACUPlus supports standard Camera Link multi-tap configurations from 8 to 64-bit/pixels. Additionally, alternate tap configurations can support up to 8 taps of 8-bits each or optionally 10 taps with alternate firmware.

DTE: Intelligent Data Transfer Engine

The X64 Xcelera-CL+ PX8 intelligent Data Transfer Engine ensures fast image data transfers between the board and the host computer with zero CPU usage. The DTE provides a high degree of data integrity during continuous image acquisition in a non-real time operating system like Windows. DTE consists of multiple independent DMA units, Tap Descriptor Tables, and Auto-loading Scatter-Gather tables.

PCI Express x8 Interface

The X64 Xcelera-CL+ PX8 is a universal PCI Express x8 board, compliant with the PCI Express 1.1 specification. The X64 Xcelera-CL+ PX8 board achieves transfer rates up to 1.5Gbytes/sec. to host memory.

The X64 Xcelera-CL+ PX8 board occupies one PCI Express x8 expansion slot and one chassis opening.

Important:

- Older computers may not support the maximum data transfer bandwidth defined for PCI Express x8. Such computers may electrically support only x4 devices even in their x8 slot. The X64 Xcelera-CL+ PX8 will function correctly in such a computer but at a lower maximum data rate.
- If the computer only has a PCI Express x16 slot, test directly or review the computer documentation to know if the X64 Xcelera-CL+ PX8 is supported. Many computer motherboards only support x16 products in x16 slots, commonly used with graphic video boards.

Advanced Controls Overview

Visual Indicators

X64 Xcelera-CL+ PX8 features 3 LED indicators to facilitate system installation and setup. These indicators provide visual feedback on the board status and camera status.

External Event Synchronization

Trigger inputs and strobe signals precisely synchronize image captures with external events.

Camera Link Communications ports

One (Full board) or two (Dual board) PC independent communication ports provide Camera Link camera configuration. These ports do not require addition PC resources like free interrupts or I/O address space. Accessible via the board device driver, the communication ports present a seamless interface to Windows-based standard communication applications like HyperTerminal, etc. The communication ports are accessible directly from the Camera Link connectors.

Quadrature Shaft Encoder

An important feature for web scanning applications, the Quadrature Shaft Encoder inputs allow synchronized line captures from external web encoders. The X64 Xcelera-CL+ PX8 provides two ways to connect a shaft encoder: (1) an opto-coupled input that supports a tick rate of up to 200 kHz and (2) an LVDS input that supports a tick rate of up to 5 MHz.

Development Software Overview

Sapera++ LT Library

Sapera++ LT is a powerful development library for image acquisition and control. Sapera++ LT provides a single API across all current and future Teledyne DALSA hardware. Sapera++ LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards. Applications are developed using either C++ or .NET frameworks.

Sapera++ LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes or .NET classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

Installing X64 Xcelera-CL+ PX8

Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation.

If you do not feel comfortable performing the installation, please consult a qualified computer technician.

Important: Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up on installation of a board.

Installation

Note: to install Sapera LT and the X64 Xcelera-CL+ PX8 device driver, logon to the workstation as administrator or with an account that has administrator privileges.

The Sapera LT Development Library (or 'runtime library' if application execution without development is preferred) must be installed before the Xcelera-CL+ PX8 device driver.

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the X64 Xcelera-CL+ PX8 into a free PCI Express x8 expansion slot. Note that some computer's x16 slot may support the X64 Xcelera-CL+ PX8.
- Close the computer chassis and turn the computer on.
- Windows will find the X64 Xcelera-CL+ PX8 and start its **Found New Hardware Wizard**. Click on the **Cancel** button to close the Wizard.
- If using **Windows Vista or Windows 7**, Windows will display its **Found New Hardware dialog**. Click on the default "*Ask me again later*" and continue with the installation. Note that if you select the third option "*Don't show this message again for this device*", there will be no prompt if the Teledyne DALSA board is installed in the same computer.

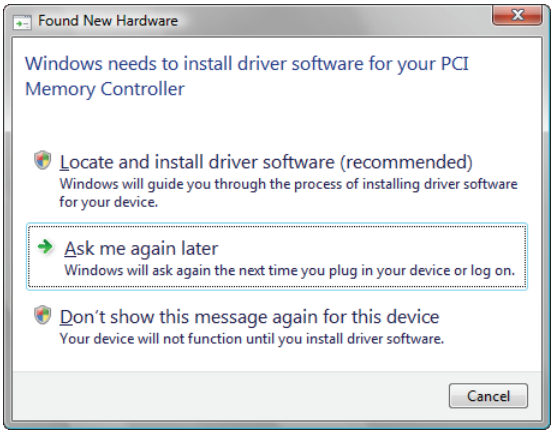

Figure 1: Found New Hardware

Sapera LT Library Installation

- Insert the Teledyne DALSA Sapera Essential CD-ROM. With **AUTORUN** enabled, the installation menu automatically displays.
- With **AUTORUN** not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu and install the required Sapera components.
- Continue with the installation of the board driver as described in the next section.
- The installation program will prompt you to reboot the computer.

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

X64 Xcelera-CL+ PX8 Driver Installation

The X64 Xcelera-CL+ PX8 board driver supports installation in a Windows XP, Windows Vista, or Windows 7 system.

- After installing Sapera, continue by selecting the X64 Xcelera-CL+ PX8 driver installation.
- If Sapera was previously installed, insert the Teledyne DALSA Sapera Essential CD-ROM to install the board driver. With **AUTORUN** enabled, the installation menu automatically displays. Install the X64 Xcelera-CL+ PX8 driver.
- With **AUTORUN** not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu and install the X64 Xcelera-CL+ PX8 driver. During the late stages of the installation, the X64 Xcelera-CL+ PX8 firmware loader application starts. See the description in the following section.
- If Windows displays any unexpected message concerning the installed board, power off the system and verify that the X64 Xcelera-CL+ PX8 is installed properly in the computer slot.

X64 Xcelera-CL+ PX8 Firmware Loader

After Windows boots, the Device Manager-Firmware Loader program automatically executes at the end of the driver installation and on every subsequent reboot of the computer. It will determine if the X64 Xcelera-CL+ PX8 requires a firmware update. If firmware is required, a dialog displays. This dialog also allows the user to load firmware for alternate operational modes of the X64 Xcelera-CL+ PX8.

***Important*:** In the very rare case of firmware loader errors please see "Recovering from a Firmware Update Error" on page 36.

Firmware Update: Automatic Mode

Click **Automatic** to update the X64 Xcelera-CL+ PX8 firmware. The **X64 Xcelera-CL+ PX8 Full** supports four firmware configurations with the default being a Full, Medium, or Base camera with Flat Field correction.

The **X64 Xcelera-CL+ PX8 Dual** board supports four firmware configurations with the default being dual Base cameras with Flat Field correction.

See "Series Key Features" on page 11 and "User Programmable Configurations" on page 11 for details on all supported modes, selected via a manual firmware update.

With multiple X64 Xcelera-CL+ PX8 boards in the system, all are updated with new firmware. If any installed X64 Xcelera-CL+ PX8 board installed in a system already has the correct firmware version, an update is not required. In the following screen shot, a single X64 Xcelera-CL+ PX8 Full board is installed and ready for a firmware upgrade.

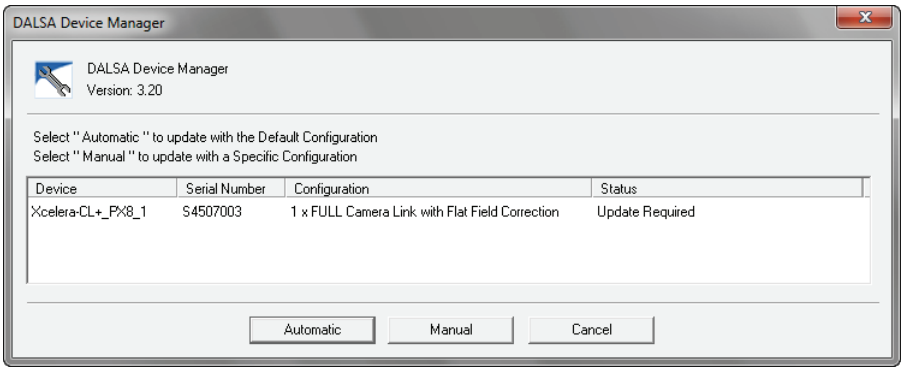

Figure 2: Automatic Firmware Update

Firmware Update: Manual Mode

Select **Manual** mode to load firmware other then the default version or when, in the case of multiple X64 Xcelera-CL+ PX8 boards in the same system, if each requires different firmware.

The following figure shows the Device Manager manual firmware screen. Displayed is information on all installed X64 Xcelera-CL+ PX8 boards, their serial numbers, and their firmware components.

Do a manual firmware update as follows:

- Select the X64 Xcelera-CL+ PX8 to update via the board selection box (if there are multiple boards in the system)
- From the Configuration field drop menu select the firmware version required
- Click on the Start Update button
- Observe the firmware update progress in the message output window
- Close the Device manager program when the device reset complete message is shown

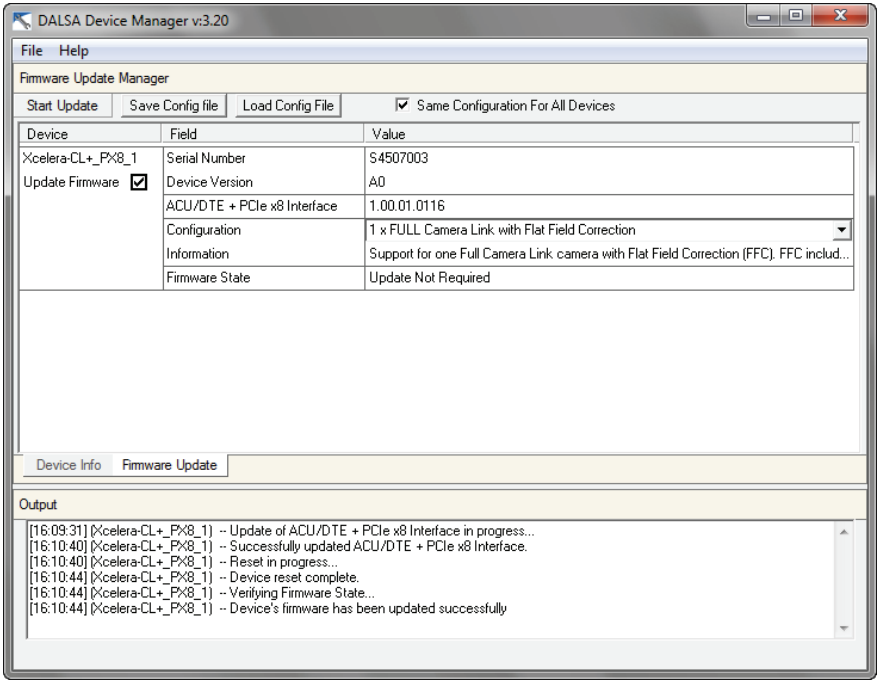

Figure 3: Manual Firmware Update

Executing the Firmware Loader from the Start Menu

If required, the X64-Xcelera-CL+ PX8 Firmware Loader program is executed via the Windows Start Menu shortcut **Start • Programs • DALSA • X64 Xcelera-CL+ PX8 Driver • Firmware Update**. A firmware change after installation would be required to select a different configuration mode. See "User Programmable Configurations" on page 11.

Requirements for a Silent Install

Both Sapera LT and the X64 Xcelera-CL+ PX8 driver installations share the same installer technology. When the installations of Teledyne DALSA products are embedded within a third party's product installation, the mode can either have user interaction or be completely silent. The following installation mode descriptions apply to both Sapera and the hardware driver.

Note: You must reboot after the installation of Sapera LT. However, to streamline the installation process, Sapera LT can be installed without rebooting before installing the board hardware device drivers. The installations then complete with a single final system reboot.

Perform Teledyne DALSA embedded installations in either of these two ways:

- **Normal Mode**
  The default mode is interactive. This is identical to running the setup.exe program manually from Windows (either run from Windows Explorer or the Windows command line).
- **Silent Mode**
  This mode requires no user interaction. A preconfigured "response" file provides the user input. The installer displays nothing.

Silent Mode Installation

A Silent Mode installation is recommended when integrating Teledyne DALSA products into your software installation. The silent installation mode allows the device driver installation to proceed without the need for mouse clicks or other input from a user.

Preparing a Silent Mode Installation requires two steps:

- Prepare the response file, which emulates a user.
- Invoke the device driver installer with command options to use the prepared response file.

Creating a Response File

Create the installer response file by performing a device driver installation with a command line switch "-r". The response file is automatically named **`setup.iss`** and is saved in the \windows folder. If a specific directory is desired, the switch –f1 is used.

As an example, to save a response file in the same directory as the installation executable of the X64 Xcelera-CL+ PX8, the command line would be:

```
X64_Xcelera-CL+_PX8_1.00.00.0000 -r -f1".\setup.iss"
```

Running a Silent Mode Installation

A device driver silent installation, whether done alone or within a larger software installation requires the device driver executable and the generated response file **`setup.iss`**.

Execute the device driver installer with the following command line:

```
X64_Xcelera-CL+_PX8_1.00.00.0000 -s -f1".\setup.iss"
```

Where the **–s** switch specifies the silent mode and the **–f1** switch specifies the location of the response file. In this example, the switch –f1".\setup.iss" specifies that the **`setup.iss`** file be in the same folder as the device driver installer.

Note: On Windows Vista and 7, the Windows Security dialog box will appear unless one has already notified Windows to 'Always trust software from "DALSA Corp." during a previous installation of a driver.

Silent Mode Uninstall

Similar to a silent installation, a response file must be prepared first as follows.

Creating a Response File

The installer response file is created by performing a device driver un-installation with a command line switch "-r". The response file is automatically named **`setup_uninstall.iss`** which is saved in the \windows folder. If a specific directory is desired, the switch "–f1" is used.

As an example, to save a response file in the same directory as the installation executable of the X64 Xcelera-CL+ PX8, the command line would be:

```
X64_Xcelera-CL+_PX8_1.00.00.0000 –r –f1".\setup_uninstall.iss"
```

Running a Silent Mode Uninstall

Similar to the device driver silent mode installation, the un-installation requires the device driver executable and the generated response file **`setup.iss`**.

Execute the device driver installer with the following command line:

```
X64_Xcelera-CL+_PX8_1.00.00.0000 -s -f1".\setup_uninstall.iss"
```

Where the **–s** switch specifies the silent mode and the **–f1** switch specifies the location of the response file. In this example, the switch –f1".\setup_uninstall.iss" specifies that the **`setup_uninstall.iss`** file be in the same folder as the device driver installer.

Silent Mode Installation Return Code

A silent mode installation creates a file “corinstall.ini” in the Windows directory. A section called [SetupResult] contains the ‘status’ of the installation. A value of 1 indicates that the installation has started and a value of 2 indicates that the installation has terminated.

A silent mode installation also creates a log file “setup.log” which by default is created in the same directory and with the same name (except for the extension) as the response file. The /f2 option enables you to specify an alternative log file location and file name, as in Setup.exe /s /f2"C:\Setup.log".

The “setup.log” file contains three sections. The first section, [InstallShield Silent], identifies the version of InstallShield used in the silent installation. It also identifies the file as a log file. The second section, [Application], identifies the installed application name, version, and the company name. The third section, [ResponseResult], contains the ‘ResultCode’ indicating whether the silent installation succeeded. A value of 0 means the installation was successful.

Installation Setup with CorAppLauncher.exe

The installation setup can be run with the CorAppLauncher.exe tool provided with the driver.

- Install the board driver and get CorAppLauncher.exe from the \bin directory of the installation.
- When running the installation, CorAppLauncher.exe will return only when the installation is finished.
- When run from within a batch file, obtain the installation exit code from the ERRORLEVEL value.
- The arguments to CorAppLauncher.exe are
  -l: Launch application
  -f: Application to launch. Specify a fully qualified path.

As an example:

- CorAppLauncher –l –f”c:\driver_install\x64_xcelera-cl+PX8_1.00.01.0100.exe”
- IF %ERRORLEVEL% NEQ 0 goto launch error

Note: There is a 32-bit and 64-bit version of CorAppLauncher.exe. When installing the driver, only the version related to the OS is installed. However, the 32-bit version is usable on either 32-bit or 64-bit Windows.

Custom Driver Installation using install.ini

Customize the driver installation by parameters defined in the file “install.ini”. By using this file, the user can:

- Select the user default configuration.
- Select different configurations for systems with multiple boards.
- Assign a standard Serial COM port to board.

Creating the install.ini File

- Install the driver in the target computer. All X64 Xcelera-CL+ PX8 boards required in the system must be installed.
- Configure each board's acquisition firmware using the Teledyne DALSA Device Manager tool (see Device Manager – Board Viewer).
- If a standard Serial COM port is required for any board, use the Sapera Configuration tool (see COM Port Assignment).
- When each board setup is complete, using the Teledyne DALSA Device Manager tool, click on the Save Config File button. This will create the "install.ini" file.

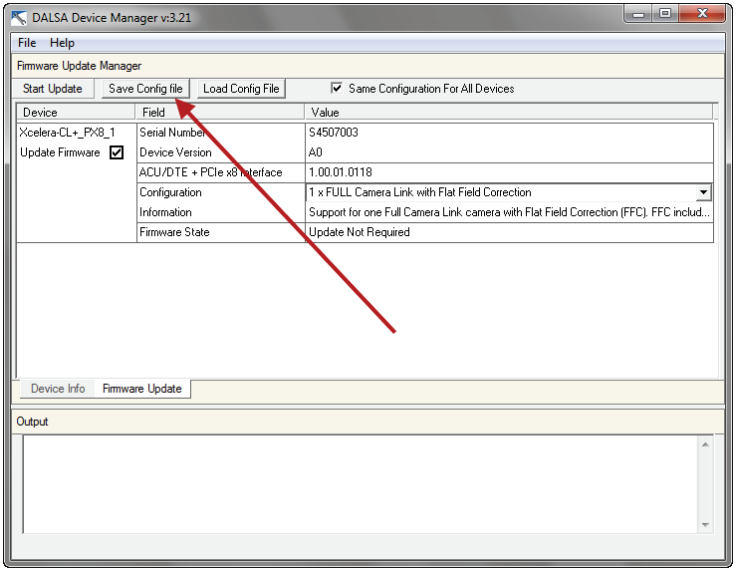

Figure 4: Create an install.ini File

Run the Installation using install.ini

Copy the install.ini file into the same directory as the setup installation file. Run the setup installation as normal. The installation will automatically check for an install.ini file and if found, use the configuration defined in it.

Upgrading Sapera or Board Driver

When installing a new version of Sapera or a Teledyne DALSA acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Described below are two upgrade situations. Note that if the board is installed in a different slot, the new hardware wizard opens. Answer as instructed in section “Installation” on page 15.

Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are distributed as ZIP files available in the Teledyne DALSA web site www.teledynedalsa.com/mv/support. Board driver revisions are also available on the next release of the Sapera Essential CD-ROM.

Often minor board driver upgrades do not require a new revision of Sapera. To confirm that the current Sapera version will work with the new board driver:

- Check the new board driver ReadMe file before installing, for information on the minimum Sapera version required.
- If the ReadMe file does not specify the Sapera version required, contact Teledyne DALSA Technical Support (see "Technical Support" on page 124).

To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows XP**, from the start menu select **Start • Settings • Control Panel • Add or Remove Programs**. Select the DALSA Xcelera board driver and click **Remove**.
- **Windows XP only:**
  - When the driver un-install is complete, reboot the computer.
  - Logon the computer as an administrator again.
- In **Windows Vista and Windows 7**, from the start menu select **Start • Settings • Control Panel • Programs and Features**. Double-click the Teledyne DALSA Xcelera board driver and click **Remove**.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.
- If the new driver is on a Sapera Essential CD-ROM follow the installation procedure described in "X64 Xcelera-CL+ PX8 Driver" on page 16.
- Important: You cannot install a Teledyne DALSA board driver without Sapera LT installed on the computer.

Upgrading both Sapera and Board Driver

When upgrading both Sapera and the acquisition board driver, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows XP**, from the start menu select **Start • Settings • Control Panel • Add or Remove Programs**. Select the Teledyne DALSA Xcelera board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- In **Windows Vista and Windows 7**, from the start menu select **Start • Settings • Control Panel • Programs and Features**. Double-click the Teledyne DALSA Xcelera board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- Reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. See "Sapera LT Library Installation" on page 16 and "X64 Xcelera-CL+ PX8 Driver" on page 16 for installation procedures.

Using the Camera Link Serial Control Port

The Camera Link cabling specification includes a serial communication port for direct camera control by the frame grabber (see "J2: Camera Link Connector 1 " on page 99). The X64 Xcelera-CL+ PX8 driver supports this serial communication port either directly or by mapping it to a host computer COM port. Any serial port communication program, such as Windows HyperTerminal, can connect to the camera in use and modify its function modes via its serial port controls. The X64 Xcelera-CL+ PX8 serial port supports communication speeds from 9600 to 115 kbps.

Note: if the serial communication program can directly select the X64 Xcelera-CL+ PX8 serial port then mapping to a system COM port is not necessary.

When required, map the X64 Xcelera-CL+ PX8 serial port to an available COM port by using the Sapera Configuration tool. Run the program from the Windows start menu: **Start • Programs • DALSA • Sapera LT • Sapera Configuration**.

COM Port Assignment

The lower section of the Sapera Configuration program screen contains the serial port configuration menu. Configure as follows:

- Use the **Physical Port** drop menu to select the Sapera board device from all available Sapera boards with serial ports (when more then one board is in the system).
- Use the **Maps to** drop menu to assign an available COM number to that Sapera board serial port.
- Click on the **Save Settings Now** button then the **Close** button. Reboot the computer at the prompt to enable the serial port mapping.
- The X64 Xcelera-CL+ PX8 serial port, now mapped to COM3 in this example, is available as a serial port to any serial port application for camera control. Note that this serial port is not listed in the **Windows Control Panel•System Properties•Device Manager** because it is a logical serial port mapping.
- An example setup using Windows HyperTerminal follows.

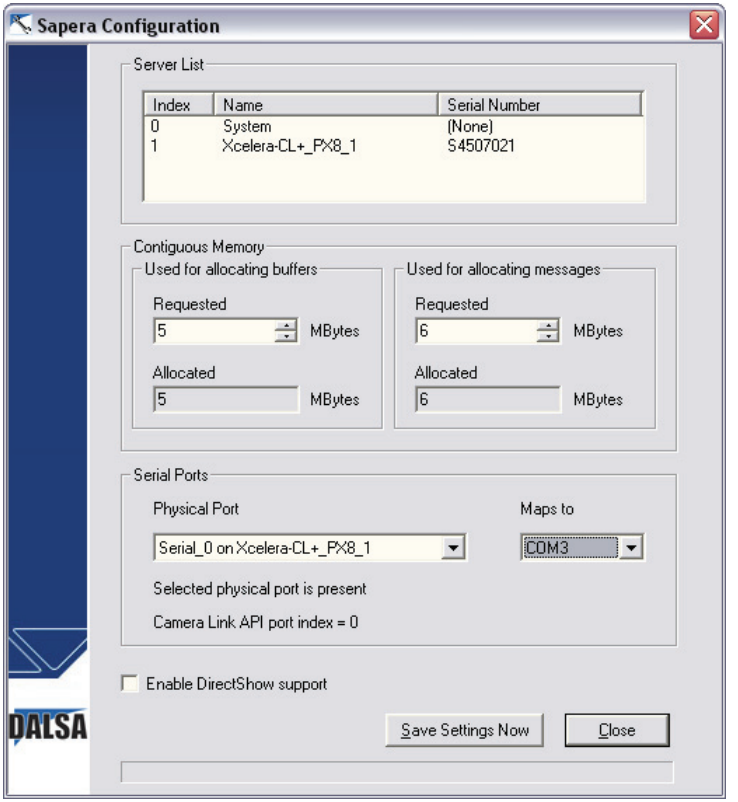

Figure 5: Sapera Configuration Program

Setup Example with Windows HyperTerminal

- Run HyperTerminal and type a name for the new connection when prompted. Then click OK.
- On the following dialog screen, select the port to connect. The port could be the COM port mapped to the X64 Xcelera-CL+ PX8 or the COM device as shown in this example.
- Note that HyperTerminal is not available in Windows Vista or Windows 7, but is available for download from various Internet locations.

Figure 6: Windows HyperTerminal Setup

- HyperTerminal now presents a dialog to configure the COM port properties. Change settings as required by the camera you are connecting. Note that the X64 Xcelera-CL+ PX8 serial port does not support hardware flow control, therefore set flow control to none.

Displaying X64 Xcelera-CL+ PX8 Board Information

The Device Manager program also displays information about the X64 Xcelera-CL+ PX8 boards installed in the system. To view board information run the program via the Windows Start Menu shortcut **Start • Programs • DALSA • X64 Xcelera-CL+ PX8 Device Driver • Device Manager**.

Device Manager – Board Viewer

The following screen image shows the Device Manager program with the Information/Firmware tab active. The left window displays all Teledyne DALSA boards in the system and their individual device components. The right window displays the information stored in the selected board device. This example screen shows the X64 Xcelera-CL+ PX8 information contained in the EEProm component.

Generate the X64 Xcelera-CL+ PX8 device manager report file (BoardInfo.txt) by clicking **File • Save Device Info**. Teledyne DALSA Technical Support may request this report to aid in troubleshooting installation or operational problems.

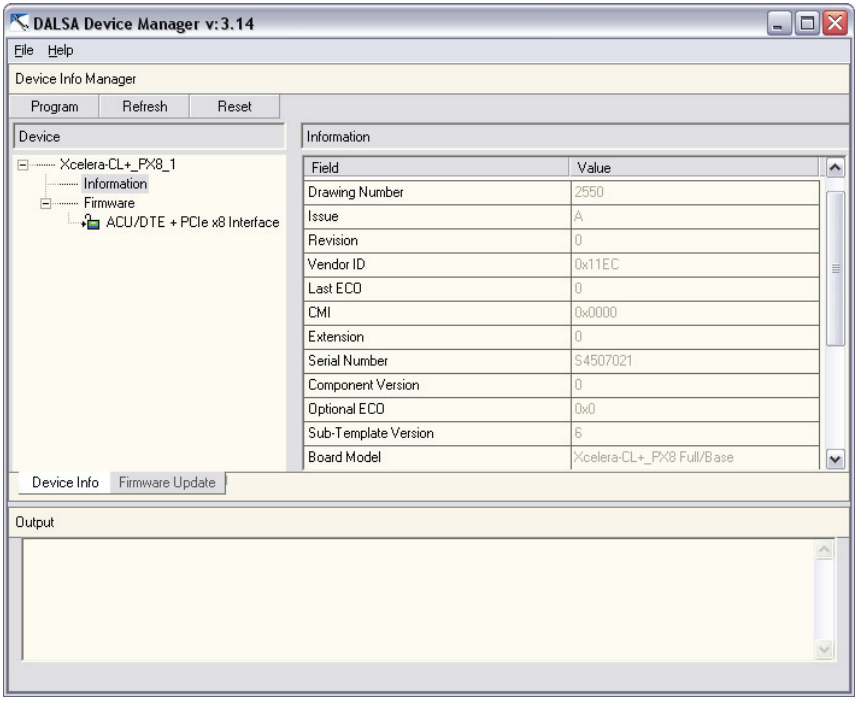

Figure 7: Board Information via Device Manager

Configuring Sapera

Viewing Installed Sapera Servers

The Sapera configuration program (**Start • Programs • DALSA • Sapera LT • Sapera Configuration**) allows the user to see all available Sapera servers for the installed Sapera-compatible boards. The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should always be present.

Increasing Contiguous Memory for Sapera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory, occupying consecutive addresses) reserved for the resources needed for **Sapera buffers** allocation and **Sapera messaging**. For both items, the **Requested** value dialog box shows the 'CorMem' driver default memory setting while the **Allocated** value displays the amount of contiguous memory allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sapera buffers** value determines the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for frame buffer management such as scatter-gather list, DMA descriptor tables plus other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers or when connecting the buffers via a transfer object. You can approximate the amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for frame buffers
  [number of frame buffers • number of pixels per line • number of lines • (2 - if buffer is 10 or 12 bits)].
- Provide 1MB for every 256 MB of frame buffer memory required.
- Add an additional 1 MB if the frame buffers have a short line length, say 1k or less
  (the increased number of individual frame buffers requires more resources).
- Add an additional 2 MB for various static and dynamic Sapera resources.
- Add the amount of memory needed for DMA tables using the formula (Sapera 7.10 and up):
  [number of frame buffers • number of lines • 16 • (line length in bytes / 4kB)].
- Test for any memory error when allocating host buffers. Simply use the Buffer menu of the Sapera Grab demo program (see "Grab Demo Overview" on page 55) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum limit of host buffers possible on your host system – the Sapera Grab demo will not crash when the requested number of host frame buffers is not allocated.

Host Computer Frame Buffer Memory Limitations

When planning a Sapera application and its host frame buffers used, plus other Sapera memory resources, do not forget the Windows operating system memory needs.

A Sapera application using the preferred *scatter gather buffers* could consume most of the remaining system memory, with a large allocation of frame buffers. If using frame buffers allocated as a *single contiguous memory block*, Windows will limit the allocation dependent on the installed system memory. Use the Buffer menu of the Sapera Grab demo program to allocate host buffer memory until an error message signals the limit allowed by the operating system used.

Contiguous Memory for Sapera Messaging

The current value for **Sapera messaging** determines the total amount of contiguous memory reserved at boot time for messages allocation. This memory space stores arguments when a Sapera function is called. Increase this value if you are using functions with large arguments, such as arrays and experience any memory errors.

Troubleshooting Problems

Overview

The X64 Xcelera-CL+ PX8 (and the X64 family of products) is tested by Teledyne DALSA in a variety of computers. Although unlikely, installation problems may occur due to the constant changing nature of computer equipment and operating systems. This section describes what the user can verify to determine the problem or the checks to make before contacting Teledyne DALSA Technical Support.

If you require help and need to contact Teledyne DALSA Technical Support, make detailed notes on your installation and/or test results for our technical support to review. See "Technical Support" on page 124 for contact information.

Problem Type Summary

X64 Xcelera-CL+ PX8 problems are either installation types where the board hardware is not recognized on the PCIe bus (i.e. trained), or function errors due to camera connections or bandwidth issues. The following links jump to various topics in this troubleshooting section.

First Step: Check the Status LED

Status LED D1 should be **GREEN** just after boot up. If it remains **RED**, the board firmware did not load correctly. If LED D1 is flashing **BLUE**, there was a PCI bus error. Refer to the Gen2 slot error described below.

Camera Link status is indicated by the two LEDs mounted between the Camera Link connectors. These LEDs show the presence of the pixel clock and an active acquisition.

The complete status LED descriptions are available in the technical reference section (see "Status LEDs Functional Description" on page 97).

Possible Installation Problems

- **Hardware PCI bus conflict:** When a new installation produces PCI bus error messages or the board driver does not install, it is important to verify that there are no conflicts with other PCI or system devices already installed. Use the Teledyne DALSA PCI Diagnostic tool as described in "Checking for PCI Bus Conflicts" on page 33. Also verify the installation via the "Windows Device Manager" on page 35.
- **Gen2 slot errors:** I have a PCI bus error message from the computer bios. Follow the instructions "GEN2 Slot Computer Issue" on page 35.
- **BSOD (blue screen) following a board reset:** After programming the board with different firmware, the computer displays the BSOD when the board is reset (see "BSOD (blue screen) Following a Board Reset" on page 35).
- **Verify Sapera and Board drivers:** If there are errors when running applications, confirm that all Sapera and board drivers are running. See "Sapera and Hardware Windows Drivers" on page 36 for details. In addition, Teledyne DALSA technical support will ask for the log file of messages by Teledyne DALSA drivers. Follow the instructions describe in "Teledyne DALSA Log Viewer" on page 38.
- **Firmware update error:** There was an error during the X64 Xcelera-CL+ PX8 firmware update procedure. The user usually easily corrects this. Follow the instructions "Recovering from a Firmware Update Error" on page 36.
- Installation went well but the board doesn't work or stopped working. Review theses steps described in "Symptoms: CamExpert Detects no Boards" on page 39.

Possible Functional Problems

- **Driver Information:** Use the Teledyne DALSA device manager program to view information about the installed X64 Xcelera-CL+ PX8 board and driver. See "Driver Information via the Device Manager Program" on page 37.
- **Area Scan Memory Requirements:** The X64 Xcelera-CL+ PX8 on board memory provides two frame buffers large enough for most imaging situations. See "Memory Requirements with Area Scan Acquisitions" on page 39 for details on the on board memory and possible limitations.

Sometimes the problem symptoms are not the result of an installation issue but due to other system issues. Review the sections described below for solutions to various X64 Xcelera-CL+ PX8 functional problems.

- "Symptoms: X64 Xcelera-CL+ PX8 Does Not Grab" on page 39
- "Symptoms: Card grabs black" on page 40
- "Symptoms: Card acquisition bandwidth is less than expected" on page 41

Troubleshooting Procedures

The following sections provide information and solutions to possible X64 Xcelera-CL+ PX8 installation and functional problems. The previous section of this manual summarizes these topics.

Checking for PCI Bus Conflicts

One of the first items to check when there is a problem with any PCI board is to examine the system PCI configuration and ensure that there are no conflicts with other PCI or system devices. The *PCI Diagnostic* program (**cpcidiag.exe**) allows examination of the PCI configuration registers and can save this information to a text file. Run the program via the Windows Start Menu shortcut **Start • Programs • DALSA • Sapera LT • Tools • PCI Diagnostics**.

As shown in the following screen image, use the first drop menu to select the PCI device to examine. Select the device from Teledyne DALSA. Note the bus and slot number of the installed board (this will be unique for each system unless systems are setup identically). Click on the **Diagnostic** button to view an analysis of the system PCI configuration space.

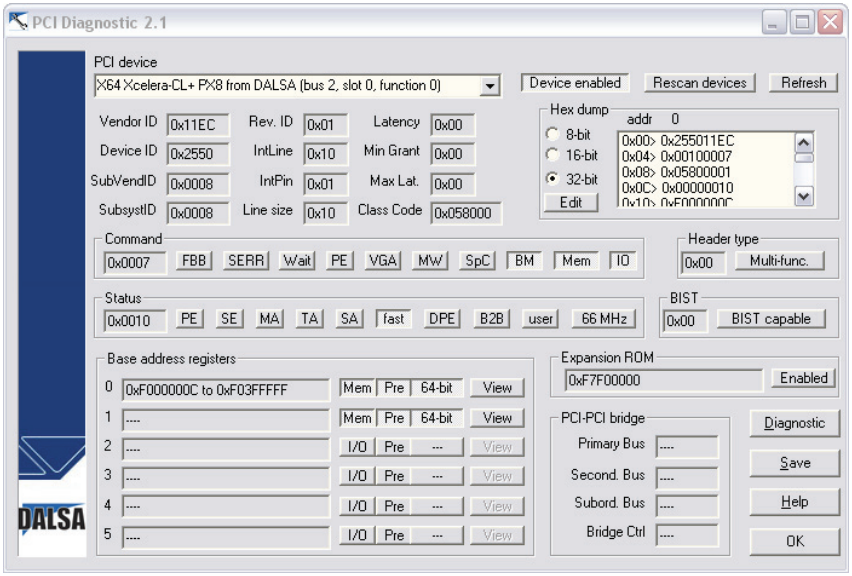

Figure 8: PCI Diagnostic Program

Clicking on the **Diagnostic** button opens a new window with the diagnostic report. From the PCI Bus Number drop menu, select the bus number that the X64 Xcelera-CL+ PX8 is installed in—in this example the slot is bus 2.

The window now shows the I/O and memory ranges used by each device on the selected PCI bus. The information display box will detail any PCI conflicts. If there is a problem, click on the **Save** button. A file named '**pcidiag.txt'** is created (in the Sapera\bin directory) with a dump of the PCI configuration registers. Email this file when requested by the Teledyne DALSA Technical Support group along with a full description of your computer.

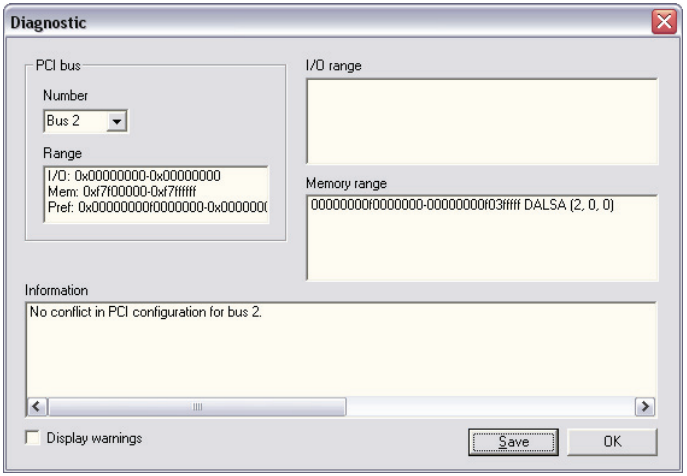

Figure 9: PCI Diagnostic Program – PCI bus info

Windows Device Manager

An alternative method to confirm the installation of the X64 Xcelera-CL+ PX8 board and driver is to use the Windows Device manager tool. Use the Start Menu shortcut **Start • Settings • Control Panel • System • Hardware • Device Manager**. As shown in the following screen images, look for *X64 Xcelera-CL+ PX8* board under “Imaging Devices”. Double-click and look at the device status. You should see “This device is working properly.” Go to “Resources” tab and make certain that the device has an interrupt assigned to it, without conflicts.

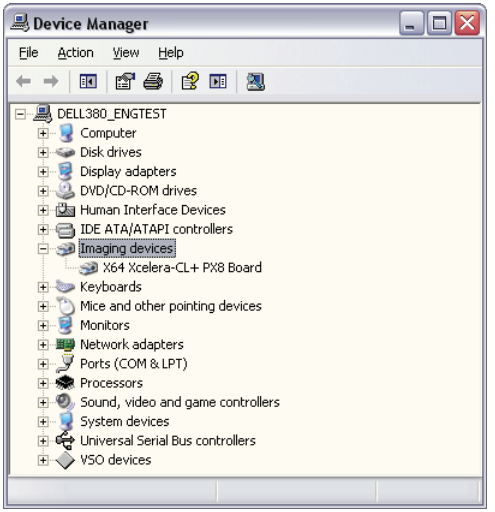

Figure 10: Using Windows Device Manager

GEN2 Slot Computer Issue

Teledyne DALSA engineering has identified cases where the X64 Xcelera-CL+ PX8 board is not detected when installed in computers using the Intel 5400 chip set. The status LED 1 flashing red identifies this issue at boot time along with a BIOS error from the computer. Change the switch SW2-2 position from the default 'OFF' to the 'ON' position before installing the Xcelera in the computer, which eliminates the PCI error. See "SW2: Normal/Safe Boot Mode & GEN2 Slot Workaround" on page 95 for details.

BSOD (blue screen) Following a Board Reset

Teledyne DALSA engineering has identified cases where a PC will falsely report a hardware malfunction when the X64 Xcelera-CL+ PX8 board is reset. The symptoms will be a Windows blue screen or PC that freezes following a board reset. The solution to this problem is to install the driver using the switch “/cr”, indicating to the driver that a reset of the board must not be allowed and that a reboot of the computer is needed instead.

- **Example**: X64_Xcelera-CL+_PX8_1.00.00.0000.exe /cr

Sapera and Hardware Windows Drivers

Any problem seen after installation, such as an error message running CamExpert, first make certain the appropriate Teledyne DALSA drivers have started successfully during the boot sequence. Example, click on the **Start • Programs • Accessories • System Tools • System Information • Software Environment** and click on **System Drivers**. Make certain the following drivers have started for the **X64 Xcelera-CL+ PX8**.

Device	Description	Type	Started
CorX64XceleraCL+PX8	X64 Xcelera-CL+ PX8 messaging	Kernel Driver	Yes
CorLog	Sapera Log viewer	Kernel Driver	Yes
CorMem	Sapera Memory manager	Kernel Driver	Yes
CorPci	Sapera PCI configuration	Kernel Driver	Yes
CorSerial	Sapera Serial Port manager	Kernel Driver	Yes

Table 4: Xcelera-CL+ PX8 Device Drivers

Teledyne DALSA Technical Support may request that you check the status of these drivers as part of the troubleshooting process.

Recovering from a Firmware Update Error

This procedure is required if any failure occurred while updating the X64 Xcelera-CL+ PX8 firmware on installation or during a manual firmware upgrade. If on the case the board has corrupted firmware, any Sapera application such as CamExpert or the grab demo program will not find an installed board to control.

Possible reasons for firmware loading errors or corruption are:

- Computer system mains power failure or deep brown-out
- PCI bus or checksum errors
- PCI bus timeout conditions due to other devices
- User forcing a partial firmware upload using an invalid firmware source file

When the X64 Xcelera-CL+ PX8 firmware is corrupted, executing a manual firmware upload will not work because the firmware loader cannot communicate with the board. In an extreme case, corrupted firmware may even prevent Windows from booting.

***Solution*:** The user manually forces the board to initialize from write-protected firmware designed only to allow driver firmware uploads. When the firmware upload is complete, reboot the board to initialize its normal operation mode.

- Note that this procedure may require removing the X64 Xcelera-CL+ PX8 board several times from the computer.
- ***Important*:** Referring to the board's user manual (in the connectors and jumpers reference section), identify the configuration switch location. The Boot Recovery Mode switch for the X64 Xcelera-CL+ PX8 is SW2-1 (see "SW2: Normal/Safe Boot Mode & GEN2 Slot Workaround" on page 95).

- Shut down Windows and power OFF the computer.
- Move the switch SW2-1 to ON, for the boot recovery mode position. (The default position is SW2-1 to OFF for normal operation).
- Power on the computer — Windows will boot normally.
- When Windows has started, do a manual firmware update procedure to update the firmware again (see "Executing the Firmware Loader from the Start Menu" on page 18).
- When the update is complete, shut down Windows and power off the computer.
- Set the SW2-1 switch back to the OFF position (i.e. default position) and power on the computer once again.
- Verify that the frame grabber is functioning by running a Sapera application such as CamExpert. The Sapera application will now be able to communicate with the X64 Xcelera-CL+ PX8 board.

Driver Information via the Device Manager Program

The Device Manager program provides a convenient method of collecting information about the installed X64 Xcelera-CL+ PX8. System information such as operating system, computer CPU, system memory, PCI configuration space, plus X64 Xcelera-CL+ PX8 firmware information is displayed or written to a text file (default file name – BoardInfo.txt). Note that this program also manually uploads firmware to the X64 Xcelera-CL+ PX8 (described elsewhere in this manual).

Execute the program via the Windows Start Menu shortcut **Start • Programs • DALSA • X64 Xcelera-CL+ PX8 Device Driver • Device Manager**. If the Device Manager Program does not run, it will exit with a board was not found message. Possible reasons for an error are:

- Board is not in the computer
- Board driver did not start or was terminated
- PCI conflict after some other device was installed

Information Window

The following figure shows the Device Manager Information screen. Click to highlight one of the board components and its information shows in the right hand window, as described below.

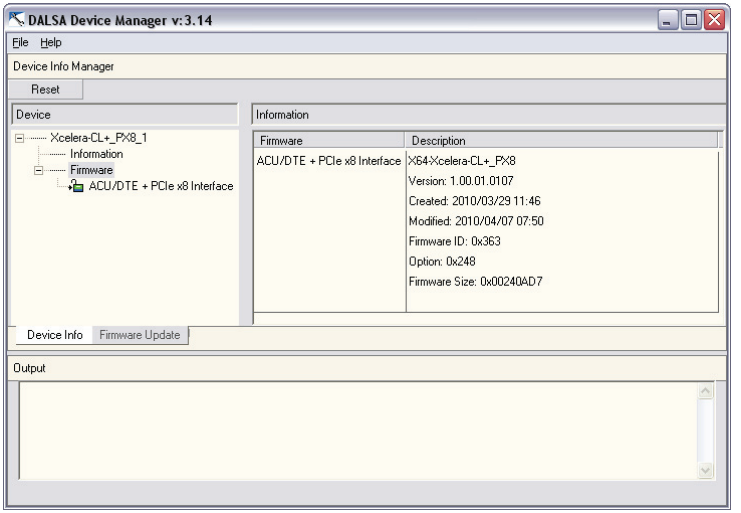

Figure 11: Board Firmware Version

- Select **Information** to display identification and information stored in the X64 Xcelera-CL+ PX8 firmware.
- Select **Firmware** to display version information for the firmware components.
- Select one of the firmware components to load *custom* firmware when supplied by Teledyne DALSA engineering for a future feature.
- Click on **File • Save Device Info** to save all information to a text file. Email this file when requested by Technical Support.

Teledyne DALSA Log Viewer

The third step in the verification process is to save in a text file the information collected by the Log Viewer program. Run the program via the Windows Start Menu shortcut **Start • Programs • DALSA • Sapera LT • Tools • Log Viewer**.

The Log Viewer lists information about the installed Teledyne DALSA drivers. Click on File • Save and you will be prompted for a text file name to save the Log Viewer contents. Email this text file to Teledyne DALSA Technical Support when requested or as part of your initial contact email.

Memory Requirements with Area Scan Acquisitions

The X64 Xcelera-CL+ PX8 allocates by default two frame buffers in on-board memory, each equal in size to the acquisition frame buffer. This double buffering memory allocation is automatic at the driver level. Two buffers will ensure that the acquired video frame is complete and not corrupted in cases where the image transfer to host system memory may be interrupted and delayed by other host system processes. That is, there is no interruption to the image acquisition of one buffer by any delays in transfer of the other buffer (which contains the previously acquired video frame) to system memory. Note that an application can change the number of on-board frame buffers using the Sapera LT API.

If allocation for the requested number of buffers fails, the driver will reduce the number of onboard frame buffers requested until they can all fit. When reaching 2 on-board buffers, if they still cannot fit, the driver will reduce the size such that it allocates two partial buffers. This mode will write image data to the buffer while wrapping image lines around to the beginning of a buffer when full. This mode relies on reading out the image data to the host computer faster than the acquisition.

Symptoms: CamExpert Detects no Boards

- When starting CamExpert, with no Teledyne DALSA board detected, CamExpert will start in offline mode. There is no error message and CamExpert is functional for creating or modifying a camera configuration file. If CamExpert should have detected the installed board, troubleshoot the installation problem as described below.

Troubleshooting Procedure

When CamExpert detects no installed Teledyne DALSA board, there could be a hardware problem, a PnP problem, a PCI problem, a kernel driver problem, or a software installation problem.

- Make certain that the card is properly seated in PCIe slot.
- Perform all installation checks described in this section before contacting Technical Support.
- Try the board in a different PCIe slot if available.

Symptoms: X64 Xcelera-CL+ PX8 Does Not Grab

You are able to start Sapera CamExpert but you do not see an image and the frame rate displayed is 0.

- Verify the camera has power.
- Verify the camera and timing parameters with the camera in free run mode.
- Verify you can grab with the camera in free run mode.
- Make certain that you provide an external trigger if the camera configuration file requires one. Use the software trigger feature of CamExpert if you do not have a trigger source.
- Verify the cable is connected to the camera.
- Make certain that the camera configuration is the required mode. This must match the camera configuration file. Refer to your camera datasheet.
- Try to snap one frame instead of continuous grab.
- Perform all installation checks described in this section before contacting Technical Support.

Symptoms: Card grabs black

You are able to use Sapera CamExpert, the displayed frame rate is as expected, but the display is always black.

- Set your camera to manual exposure mode and set the exposure to a longer period, plus open the lens iris.
- Try to snap one frame instead of continuous grab.
- Make certain that the input LUT is not programmed to output all ‘0’s.
- A PCIe transfer issue sometimes causes this problem. No PCIe transfer takes place, so the frame rate is above 0 but nevertheless no image is displayed in CamExpert.
- Make certain that BUS MASTER bit in the PCIe configuration space is activated. Look in PCI Diagnostics for **BM** button under “Command” group. Make certain that the **BM** button is activated.

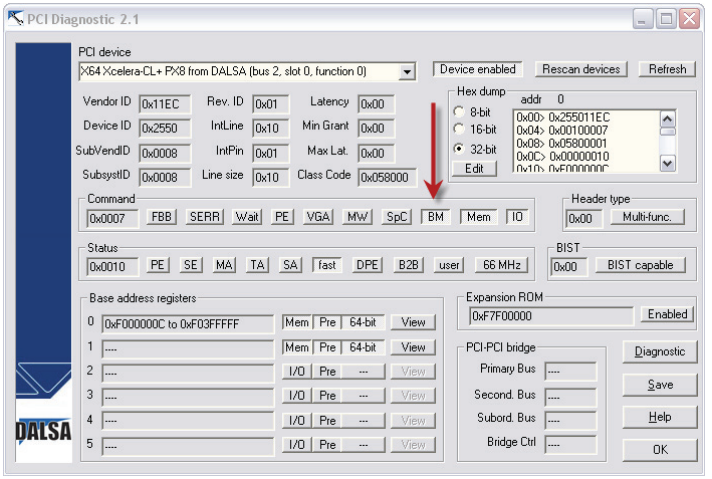

Figure 12: PCI Diagnostic – checking the BUS Master bit

- Perform all installation checks described in this section before contacting Technical Support.

Symptoms: Card acquisition bandwidth is less than expected

The X64 Xcelera-CL+ PX8 acquisition bandwidth is less than expected.

- Review the system for problems or conflicts with other expansion boards or drivers.
- Remove other PCI Express, PCI-32 or PCI-64 boards and check acquisition bandwidth again. Engineering has seen this case where other PCI boards in some systems cause limitations in transfers. Each system, with its combination of system motherboard and PCI boards, will be unique and must be tested for bandwidth limitations affecting the imaging application.
- Is the X64 Xcelera-CL+ PX8 installed in a PCI Express x16 slot?
  Note that some computer's x16 slot may only support non x16 boards at x1 or not at all. Check the computer documentation or test an X64 Xcelera-CL+ PX8 installation. The speed at which the board is running at is logged in the LogViewer. Check for an entry similar to this:
  "…X64_FPGA_GetPciSpeed = x8…"

CamExpert Quick Start

Interfacing Cameras with CamExpert

CamExpert is the camera-interfacing tool for frame grabber boards supported by the Sapera library. CamExpert generates the Sapera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. For backward compatibility with previous versions of Sapera, CamExpert also reads and writes the *.cca and *.cvi camera parameter files.

Every Sapera demo program starts by a dialog window to select a camera configuration file. Even when using the X64 Xcelera-CL+ PX8 with common video signals, a camera file is required. Therefore, CamExpert is typically the first Sapera application run after an installation. Obviously existing .ccf files can be copied to the new installation when similar cameras are used.

CamExpert Example with a Monochrome Camera

The image below shows CamExpert controlling the X64 Xcelera-CL+ PX8 Full. The camera outputs monochrome 8-bit video on a Camera Link interface. After selecting the camera model, the timing parameters are displayed and the user can test by clicking on *Grab*. Descriptions of the CamExpert windows follow the image.

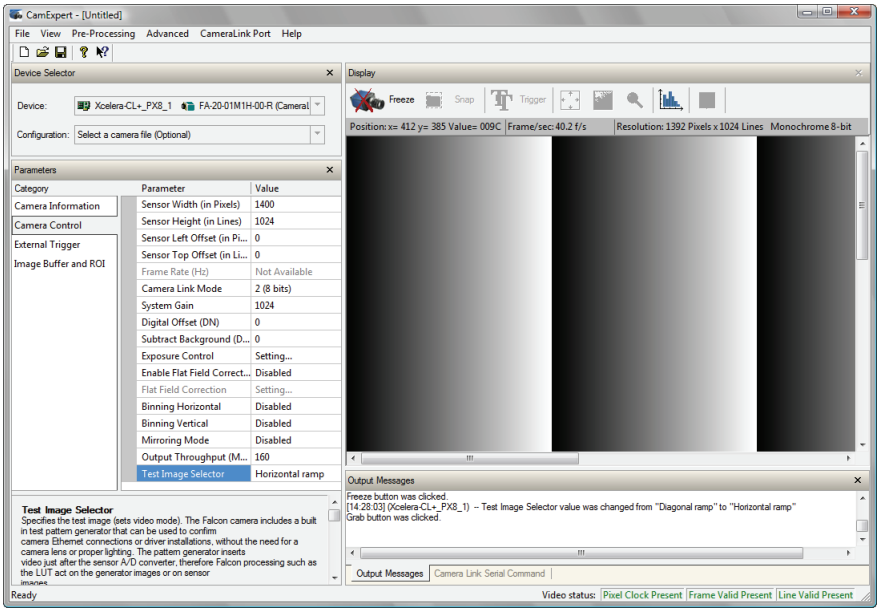

Figure 13: CamExpert Program

CamExpert groups parameters into functional categories. The parameters shown depend on the frame grabber used and what camera is connected. The parameter values are either the camera defaults or the last stored value when the camera was used. The descriptions below are with the Xcelera-CL+ PX8 and the Teledyne DALSA Falcon camera.

- **Device Selector:** Two drop menus to select which device and which saved configuration to use.
  - **Device:** Select which acquisition device to control and configure a camera file. Required in cases where there are multiple boards in a system and when one board supports multiple acquisition types. Note in this example, the installed X64 Xcelera-CL+ PX8 has firmware to support a monochrome Camera Link camera.
  - **Configuration:** Select the timing for a specific camera model included with the Sapera installation or a standard video standard. The *User's* subsection is where user created camera files are stored.

- **Parameter Groups:** Select a function category and change parameter values as required. Descriptions for the camera parameters change dependent on the camera. The following information pertains to a Teledyne DALSA Falcon camera.
  - **Camera Information:** Provides static camera parameters along with a dialog to save a user setup.
  - **Camera Control:** Basic and advanced parameters used to define the timing and pixel type of the camera. Select the pixel mode, Horizontal active resolution, Vertical Resolution (for area scan sensors), Pixel Clock frequency, Camera sensor readout type, Binning, etc. dependent on the camera used. This group is sufficient to configure a free-running camera.
  - **External Trigger:** Parameters to configure the external trigger characteristics.
  - **Image Buffer and ROI:** Allows control of the host buffer dimension and format.

- **Display:** An important component of CamExpert is its live acquisition display window, which allows immediate verification of timing or control parameters without the need to run a separate acquisition program. **Grab** starts continuous acquisition (button then toggles to **Freeze** to stop). **Snap** is a single frame grab. **Trigger** is a software trigger to emulate an external source.
- **Output Messages and Video Status Bar:** Events and errors are logged for review. Camera connection status is displayed where green indicates signal present.
- **Camera Link Serial Command:** Select this Tab to open a serial command port to the camera. This allows the user to issue configuration commands if supported by the camera.

For context sensitive help click on the  button then click on a camera configuration parameter. A popup provides a short description of the configuration parameter. Click on the  button to open the help file for more descriptive information on CamExpert.

CamExpert Demonstration and Test Tools

The CamExpert utility also includes a number of demonstration features, which make CamExpert the primary tool to configure, test and calibrate your camera and imaging setup. Display tools include, image pixel value readout, image zoom, and line profiler.

Functional tools include hardware Flat Field calibration and operation support (see "X64 Xcelera-CL+ PX8 Flat Field/Flat Line Support" on page 48), plus support for either hardware based or software Bayer filter camera decoding with auto white balance calibration (see "Using the Bayer Filter Tool" on page 52).

Camera Types & Files

The X64 Xcelera-CL+ PX8 supports digital area scan or line scan cameras using the Camera Link interface standard. Contact Teledyne DALSA or browse our web site [www.teledynedalsa.com] for the latest information and application notes on X64 Xcelera-CL+ PX8 supported cameras.

Camera Files Distributed with Sapera

The Sapera distribution CDROM includes camera files for a selection of X64 Xcelera-CL+ PX8 supported cameras. Using the Sapera CamExpert program, you may use the camera files (CCA) provided to generate a camera configuration file (CCF) that describes the desired camera and frame grabber configuration..

Teledyne DALSA continually updates a camera application library composed of application information and prepared camera files. Camera files are ASCII text, readable with Windows Notepad on any computer without having Sapera installed.

Overview of Sapera Acquisition Parameter Files (*.ccf or *.cca/*.cvi)

Concepts and Differences between the Parameter Files

There are two components to the legacy Sapera acquisition parameter file set: CCA files (also called cam-files) and CVI files (also called VIC files, i.e. video input conditioning). The files store video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplifies programming the frame-grabber acquisition hardware for the camera in use. **Sapera LT 5.0** introduces a new camera configuration file (**CCF**) that combines the CCA and CVI files into one file.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera-operating mode). An application can also have multiple CCA/CCF files to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

CCF File Details

A file using the ".CCF" extension, (Camera Configuration files), is the camera (CCA) and frame grabber (CVI) parameters grouped into one file for easier configuration file management. This is the default Camera Configuration file used with Sapera LT 5.0 and the CamExpert utility.

CCA File Details

Teledyne DALSA distributes camera files using the legacy ".CCA" extension, (CAMERA files), which contain all parameters describing the camera video signal characteristics and operation modes (what the camera outputs). The Sapera parameter groups within the file are:

- Video format and pixel definition
- Video resolution (pixel rate, pixels per line, lines per frame)
- Synchronization source and timing
- Channels/Taps configuration
- Supported camera modes and related parameters
- External signal assignment

CVI File Details

Legacy files using the ".CVI" extension contain all operating parameters related to the frame grabber board - what the frame grabber can actually do with camera controls or incoming video. The Sapera parameter groups within the file are:

- Activate and set any supported camera control mode or control variable.
- Define the integration mode and duration.
- Define the strobe output control.
- Allocate the frame grabber transfer ROI, the host video buffer size and buffer type (RGB888, RGB101010, MONO8, and MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, RS-422, OPTO-isolated), and signal active edge or level characterization.

Saving a Camera File

Use CamExpert to save a camera file (*.ccf) usable with any Sapera demo program or user application. An example would be a camera file, which sets up parameters for a free running camera (i.e. internal trigger) with exposure settings for a good image with common lighting conditions.

When CamExpert is setup as required, click on **File•Save As** to save the new .ccf file. The dialog that opens allows adding details such as camera information, mode of operation, and a file name for the .ccf file. The following image is a sample for a Teledyne DALSA Falcon camera. Note the default folder where User camera files are saved.

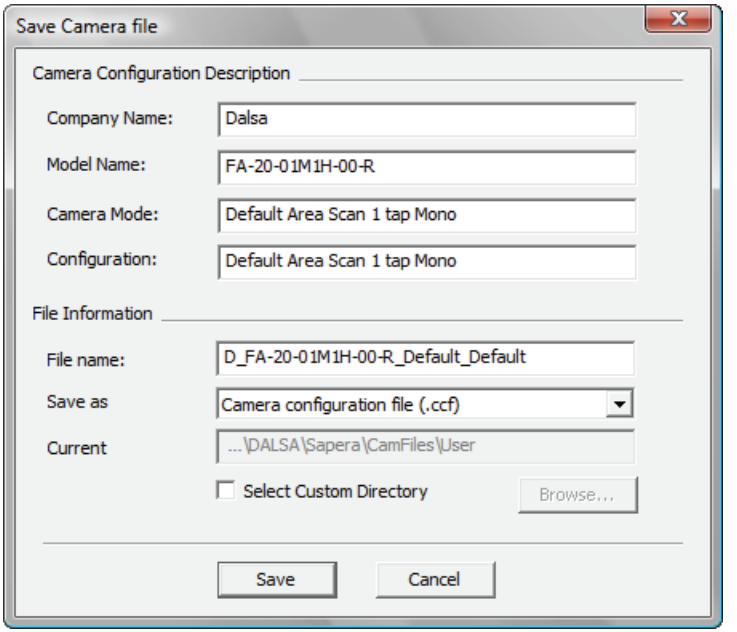

Figure 14: Saving a New Camera File (.ccf)

Camera Interfacing Check List

Before interfacing a camera from scratch with CamExpert:

- Confirm that Teledyne DALSA has not already published an application note with camera files [www.teledynedalsa.com].
- Confirm that the correct version or board revision of X64 Xcelera-CL+ PX8 is used. Confirm that the required firmware is loaded into the X64 Xcelera-CL+ PX8.
- Confirm that Sapera does not already have a .cca file for your camera installed on your hard disk. If there is a .cca file supplied with Sapera, then use CamExpert to generate the .ccf file with default parameter values matching the frame grabber capabilities.
- Check if the Sapera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert and modified to match timing and operating parameters for your camera, and lastly save them as Camera Configuration file (.ccf).
- Finally, if there is no file for your camera, run CamExpert after installing Sapera and the acquisition board driver, select the board acquisition server, and manually enter the camera parameters.

X64 Xcelera-CL+ PX8 Flat Field/Flat Line Support

The X64 Xcelera-CL+ PX8 supports hardware based real-time Flat Field Correction. The default firmware for the Full or Dual version board supports flat field correction. See "User Programmable Configurations" on page 11 for information on driver versions.

Flat Field Correction is the process of eliminating small gain differences between pixels in a sensor array. That sensor when exposed to a uniformly lit field will have no gray level differences between pixels when applying the calibrated flat field correction to the image. The CamExpert Flat Field tool functions with hardware supporting flat field processing.

Loading the Required Camera File

Select the required camera configuration file for the connected camera. Verify the acquisition with the live grab function. Make camera adjustments to get good images.

Set up Dark and Bright Acquisitions with the Histogram Tool

Before performing calibration, verify the acquisition with a live grab. Also at this time, make preparations to grab a flat light gray level image, required for the calibration, such as a clean evenly lighted white wall or non-glossy paper with the lens slightly out of focus. Ideally, a controlled diffused light source aimed directly at the lens is used. Note the lens iris position for a bright but not saturated image. Additionally check that the lens iris closes well or have a lens cover to grab the dark calibration image.

Verify a Dark Acquisition

Close the camera lens iris and cover the lens with a lens cap. Using CamExpert, click on the grab button and then the histogram button. The following figure shows a typical histogram for a very dark image.

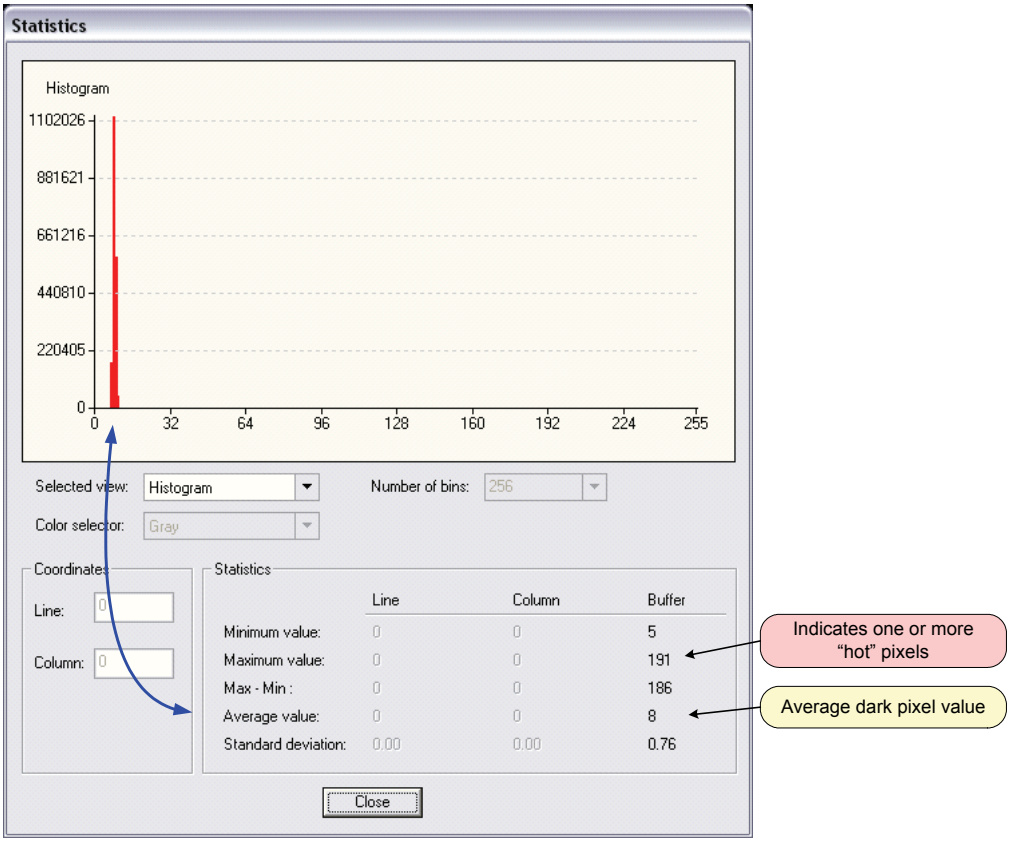

Figure 15: Flat Field - Verify a Dark Acquisition

Important: In this example, the **average** pixel value for the frame is close to black. Also, note that most sensors will show a much higher maximum pixel value due to one or more "hot pixels". The sensor specification accounts for a small number of hot or stuck pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

Verify a Bright Acquisition

Aim the camera at a diffused light source or evenly lit white wall with no shadows falling on it. Using CamExpert, click on the grab button and then the histogram button. Use the lens iris to adjust for a bright gray approximately around a pixel value of 200 (for 8-bit pixels). The following figure shows a typical histogram for a bright gray image.

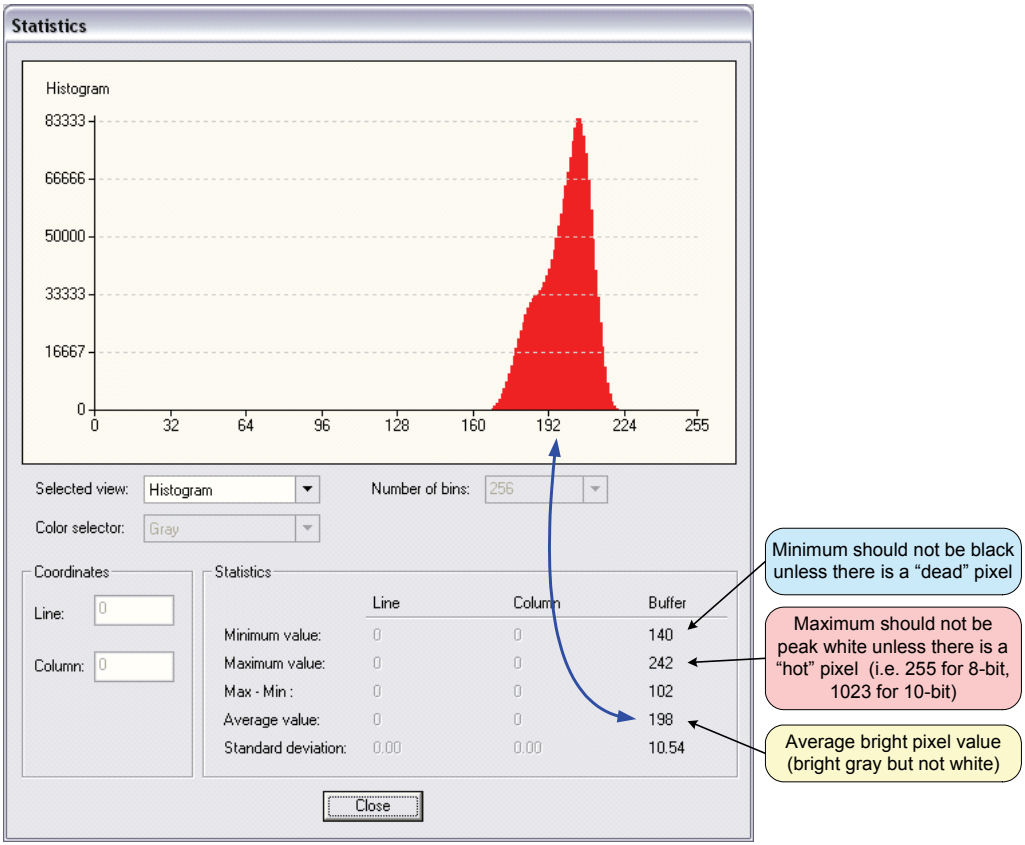

Figure 16: Flat Field - Verify a Bright Acquisition

Important: In this example, the **average** pixel value for the frame is bright gray. Also, note that sensors may show a much higher maximum or a much lower minimum pixel value due to one or more "hot or dead pixels". The sensor specification accounts for a small number of hot, stuck, or dead pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

Once the bright gray acquisition setup is done, note the camera position and lens iris position so as to be able to repeat it during the calibration procedure.

Flat Field Correction Calibration Procedure

Calibration is the process of taking two reference images, one of a black field – one of a light gray field (not saturated), to generate correction data for images captured by the CCD. Each CCD pixel data is modified by the correction factor generated by the calibration process, so that each pixel now has an identical response to the same illumination.

Start the Flat Field calibration tool via the CamExpert menu bar:
Tools • Flat Field Correction • Calibration.

Flat Field Calibration Window

The Flat Field calibration window provides a three-step process to acquire two reference images and then save the flat field correction data for the camera used. To aid in determining if the reference images are valid, use the histogram tool to review the images used for the correction data.

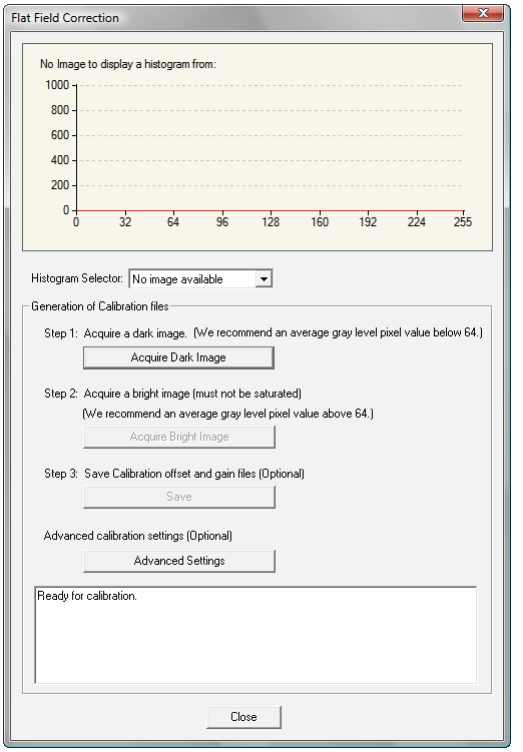

Figure 17: Flat Field – Calibration Application

- Setup the camera to capture a uniform black image. Black paper with no illumination and the camera lens' iris closed to minimum can provide such a black image.
- Click on **Acquire Black Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The desired black reference image should have pixel values less then 20. If acceptable, accept the image as the black reference.
- Setup the camera to acquire a uniform white image (but not saturated white). Even illumination on white paper is acceptable, to provide a gray level of 128 minimum. It is preferable to prepare for the white level calibration before the calibration procedure as described in the previous section.
- Click on **Acquire White Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The captured gray level for all pixels should be greater than 128. If acceptable, accept the image as the white reference.
- Click on **Save**. The flat field correction data, saved as a TIF image, is given a file name of your choice (such as camera name and serial number).

Using Flat Field Correction

From the CamExpert menu, enable Flat Field correction (**Tools • Flat Field Correction • Enable**). Now when doing a live grab or snap, the incoming image is corrected by the current flat field calibration data for each pixel.

Use the menu function **Tools • Flat Field Correction • Load** to load in a flat field correction image from a previous saved calibration data. CamExpert allows saving and loading calibration data for all cameras used with the imaging system.

Using the Bayer Filter Tool

CamExpert supports the use of Bayer Filter cameras by providing a tool to select the Bayer filter mosaic pattern and to perform an auto white balance. Manually fine tune color calibration with the RGB gain and gamma adjustments.

The CamExpert Bayer filter tool supports using either software or hardware based decoding. With boards that have Bayer filter decoding in hardware such as the X64 Xcelera-CL+ PX8 (requires loading the Bayer Decoder firmware), CamExpert directly controls the hardware for high performance real-time acquisitions from Bayer filter cameras. When standard acquisition boards are used, CamExpert performs software Bayer filter decoding using the host system processor.

Bayer Filter White Balance Calibration Procedure

The following procedure uses an X64 Xcelera-CL+ PX8 with hardware Bayer filter support (load firmware "Full Camera Link with Bayer Decoding") and any supported Bayer color camera. Use CamExpert to generate a camera file with correct camera timing parameters.

- From the CamExpert menu bar, click on **Tools • Bayer Filter**, the following menu should show **Hardware** selected by default when the X64 Xcelera-CL+ PX8 has Bayer support.
- Select **Setting** to access the color calibration window (see following figure).

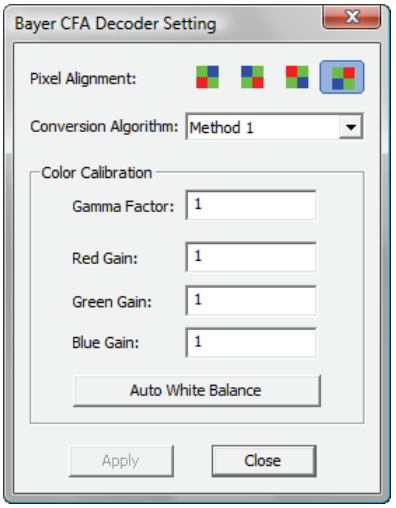

Figure 18: Bayer White Balance Calibration

- Click **Grab** to start live acquisition.
- Aim and focus the camera on an area of white or a large sheet of white paper in front of the object.
- Click on one of the four Bayer pixel alignment patterns to match the camera (best color before calibration). Typically, the CamExpert default is correct for a majority of cameras.
- Adjust the lens iris to reduce the exposure brightness so that the white image area is now darker. Make certain that no pixel in the white area is saturated.
- Use the mouse left button, click and drag a ROI enclosing a portion of the white area.
- Click on the **Auto White Balance** button. CamExpert will make RGB gain adjustments.
- Open the camera iris to have a correctly exposed image.
- Review the image for color balance.
- Manually make additional adjustments to the RGB gain values. Fine-tune the color balance to achieve best results. Adjust the gamma factor to improve the display.
- Stop the live acquisition and save the camera file (which now contains the Bayer RGB calibration information). Note that the gamma factor is not saved because it is not a Sapera parameter but only a display tool.

Using the Bayer Filter

A Sapera application, when loading the camera file parameters, will have the RGB gain adjustment values. The application can provide the calibration window to make RGB adjustments as required.

Sapera Demo Applications

Grab Demo Overview

Program	**Start•Programs•DALSA•Sapera LT•Demos•Frame Grabbers•Grab Demo**
Program file	**…\...\Sapera\Demos\Classes\vc\GrabDemo\Release\GrabDemo.exe**
Workspace	**…\...\Sapera\Demos\Classes\vc\SapDemos.dsw**
.NET Solution	**…\...\Sapera\Demos\Classes\vc\SapDemos_2003.sln** **…\...\Sapera\Demos\Classes\vc\SapDemos_2005.sln** **…\...\Sapera\Demos\Classes\vc\SapDemos_2008.sln** **…\...\Sapera\Demos\Classes\vc\SapDemos_2010.sln**
Description	This program demonstrates the basic acquisition functions included in the Sapera library. The program either allows you to acquire images, in continuous or in one-time mode, while adjusting the acquisition parameters. The program code may be extracted for use within your own application.
Remarks	This demo is built using Visual C++ 6.0. It is based on Sapera C++ classes. See the Sapera User's and Reference manuals for more information.

Table 5: Grab Demo Workspace Details

Using the Grab Demo

Server Selection

Run the grab demo from the start menu **Start•Programs•Sapera LT•Demos•Frame Grabbers•Grab Demo**.

The demo program first displays the acquisition configuration menu. The first drop menu displayed permits selecting from any installed Sapera acquisition servers (installed Teledyne DALSA acquisition hardware using Sapera drivers). The second drop menu permits selecting from the available input devices present on the selected server.

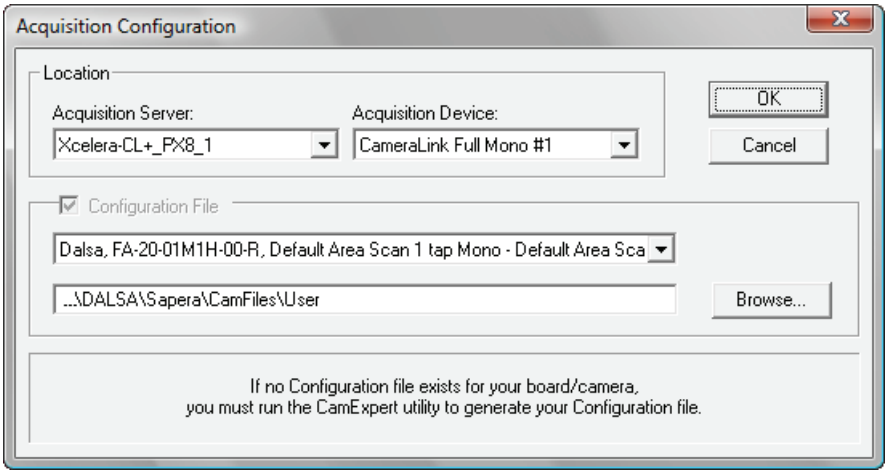

Figure 19: Grab Demo – Server Selection

CCF File Selection

Use the acquisition configuration menu to select the required camera configuration file for the connected camera. Sapera camera files contain timing parameters and video conditioning parameters. The default folder for camera configuration files is the same used by the CamExpert utility to save user generated or modified camera files.

Use the Sapera CamExpert utility program to generate the camera configuration file based on timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of those parameters. CamExpert reads both Sapera *.cca and *.cvi for backward compatibility with the original Sapera camera files.

Grab Demo Main Window

The Grab Demo program provides basic acquisition control for the selected frame grabber. The loaded camera file (.ccf) defines the Frame buffer defaults.

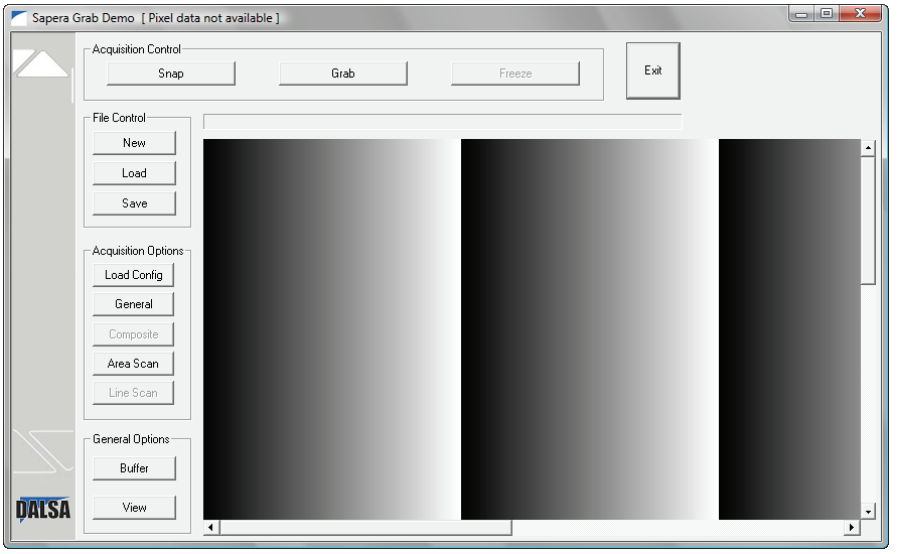

Figure 20: Grab Demo Main Window

Refer to the Sapera LT User's Manual (OC-SAPM-USER), in section "Demos and Examples – Acquiring with Grab Demo", for more information on the Grab Demo.

Flat-Field Demo Overview

Program	**Start•Programs•DALSA•Sapera LT•Demos•Frame Grabbers•Flat Field Demo**
Program file	**…\...\Sapera\Demos\Classes\vc\FlatFieldDemo\Release\FlatfieldDemo.exe**
Workspace	**…\...\Sapera\Demos\Classes\vc\SapDemos.dsw**
Description	This program demonstrates Flat Field or Flat Line processing, either performed by supporting Teledyne DALSA hardware or performed on the host system via the Sapera library. The program allows you to acquire a flat field or flat line reference image, and then do real time correction either in continuous or single acquisition mode. The program code may be extracted for use within your own application.
Remarks	This demo is built using Visual C++ 6.0. It is based on Sapera C++ classes. See the Sapera User's and Reference manuals for more information.

Table 6: Flat-Field Demo Workspace Details

Using the Flat Field Demo

Refer to the Sapera LT User's Manual (OC-SAPM-USER), in section "Using the Flat Field Demo", for more information.

X64 Xcelera-CL+ PX8 Reference

Full Block Diagram

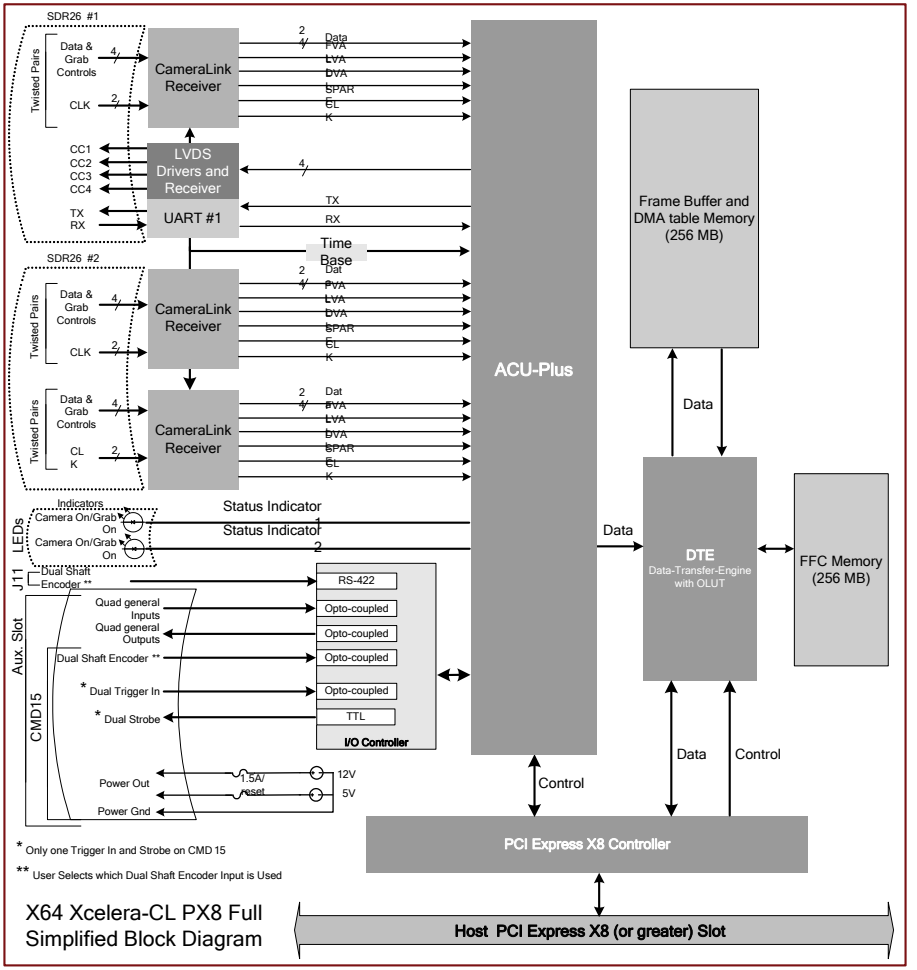

Figure 21: Full Model Block Diagram

Acquisition Timing

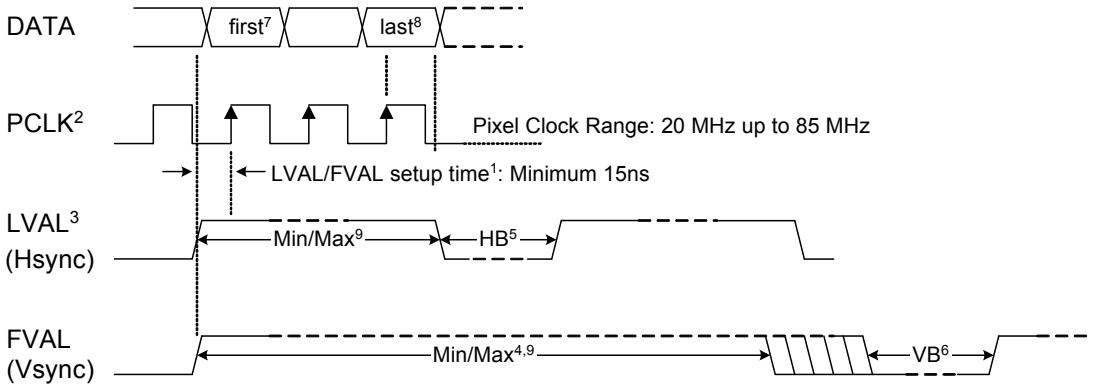

Figure 22: Acquisition Timing

- [1] The setup times for LVAL and FVAL are the same. Both must be high and stable before the rising edge of the Pixel Clock.
- [2] Pixel Clock must always be present
- [3] LVAL must be active high to acquire camera data
- [4] Minimum of 1
- [5] HB - Horizontal Blanking:

Minimum:	4 clock cycles
Maximum:	no limits

- [6] VB - Vertical Blanking:

Minimum:	1 line
Maximum:	no limits

- [7] First Active Pixel (unless otherwise specified in the CCA file – "Horizontal Back invalid = x" where 'x' defines the number of pixels to be skipped).
- Note: If HB is less than 4 clock cycles, HB will be extended to 4 clock cycles. The number of clock cycles used to extend to 4 will reduce the number of active pixels acquired accordingly.
- [8] Last Active Pixel – defined in the CCA file under "Horizontal active = y" – where 'y' is the total number of active pixels per tap.
- [9] Maximum Valid Data:
  - 8-bits/pixel x 16 Million Pixels/line (LVAL)
  - 16-bits/pixel x 8 Million Pixels/line (LVAL)
  - 32-bits/pixel x 4 Million Pixels/line (LVAL)
  - 64-bits/pixel x 2 Million Pixels/line (LVAL)
  - 16 Million lines (FVAL)

Table 7: Acquisition Timing Specifications

Line Trigger Source Selection for Line scan Applications

Line scan imaging applications require some form of external event trigger to synchronize line scan camera exposures to the moving object. This synchronization signal is either an external trigger source (one exposure per trigger event) or a shaft encoder source composed of a single or dual phase (also known as a quadrature) signal.

The X64 Xcelera-CL+ PX8 shaft encoder inputs provide additional functionality with pulse drop, pulse multiply, and pulse direction support, along with error trapping event notifications such as "*External Line Trigger Too Fast*" (see "Supported Events and Transfer Methods" on page 68).

When using the shaft encoder signals, the user can choose to connect to the opto-coupled inputs or the RS422/TTL inputs (which support a higher maximum pulse frequency). The imaging application chooses which shaft encoder input to use via a board parameter (described following the table below).

The following table describes the line-trigger source types supported by the X64 Xcelera-CL+ PX8. Refer to the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00) for descriptions of the Sapera parameters.

CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE – Parameter Values Specific to the X64-Xcelera-CL+ PX8

PRM Value	X64 Xcelera-CL+ PX8 configuration & camera input used	Input used as: External Line Trigger	Input used as: External Shaft Encoder
		if CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE = *true*	*if* CORACQ_PRM_SHAFT_ENCODER_ENABLE =*true*
0	Dual - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
	Dual - Camera #2	Shaft Encoder Phase B	Shaft Encoder Phase B
	Full - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A & B
1	Dual - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
	Dual - Camera #2	Shaft Encoder Phase A	Shaft Encoder Phase A
	Full - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
2	Dual - Camera #1	Shaft Encoder Phase B	Shaft Encoder Phase B
	Dual - Camera #2	Shaft Encoder Phase B	Shaft Encoder Phase B
	Full - Camera #1	Shaft Encoder Phase B	Shaft Encoder Phase B

3, 5, 6, 7	Dual - Camera #1	n/a	Shaft Encoder Phase A & B
	Dual - Camera #2	n/a	Shaft Encoder Phase A & B
	Full - Camera #1	n/a	Shaft Encoder Phase A & B
4	Dual - Camera #1	From Board Sync	From Board Sync
	Dual - Camera #2	From Board Sync	From Board Sync
	Full - Camera #1	From Board Sync	From Board Sync

Table 8: CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE – Parameter Values

See "J4: External Signals Connector " on page 102 for shaft encoder input connector details.

CVI/CCF File Parameters Used

- External Line Trigger Source = prm value
- External Line Trigger Enable = true/false
- Shaft Encoder Source = X, where:
  - If X = 0, Shaft Encoder selection is done automatically by the driver. In this case, the opto-coupled input circuit is selected.
  - If X = 1, opto-coupled Shaft Encoder
  - If X = 2, RS-422 Shaft Encoder
- Shaft Encoder Enable = true/false

Shaft Encoder Interface Timing

Dual Balanced Shaft Encoder Opto-Coupled Inputs:

- Input Phase A
  - Connector J1: Pin 2 (Phase A +) & Pin 10 (Phase A -)
  - Connector J4: Pin 23 (Phase A +) & Pin 24 (Phase A -)
- Input Phase B
  - Connector J1: Pin 3 (Phase B+) & Pin 11 (Phase B-)
  - Connector J4: Pin 25 (Phase B +) & Pin 26 (Phase B -)
- See “External Signals Connector Bracket Assembly” on page 109 for pinout information about the DB37 used for external connections.
- See "J1 CMD15 Female External Signals Connector Descriptions" on page 103 for complete connector signal details)
- See "J4: External Signals Connector " on page 102 for complete connector signal details)

Dual Balanced Shaft Encoder RS-422 Inputs:

- Input Phase A
  - Connector J11: Pin 3 (Phase A +) & Pin 4 (Phase A -)
- Input Phase B
  - Connector J11: Pin 7 (Phase B+) & Pin 8 (Phase B-)
- See "J11: RS-422 Shaft Encoder Input" on page 116 for complete connector signal details)

Web inspection systems with variable web speeds typically provide one or two synchronization signals from a web mounted encoder to coordinate trigger signals. These trigger signals are used by the acquisition linescan camera. The X64 Xcelera-CL+ PX8 supports single or dual phase shaft encoder signals. Dual encoder signals are typically 90 degrees out of phase relative to each other and provide greater web motion resolution.

Example using any Encoder Input with Pulse-drop Counter

When enabled, the triggered camera acquires one scan line for each shaft encoder pulse-edge. To optimize the web application, a second Sapera parameter defines the number of triggers to skip between valid acquisition triggers. The figure below depicts a system where a valid camera trigger is any pulse edge from either shaft encoder signal. After a trigger, the two following triggers are ignored (as defined by the Sapera pulse drop parameter).

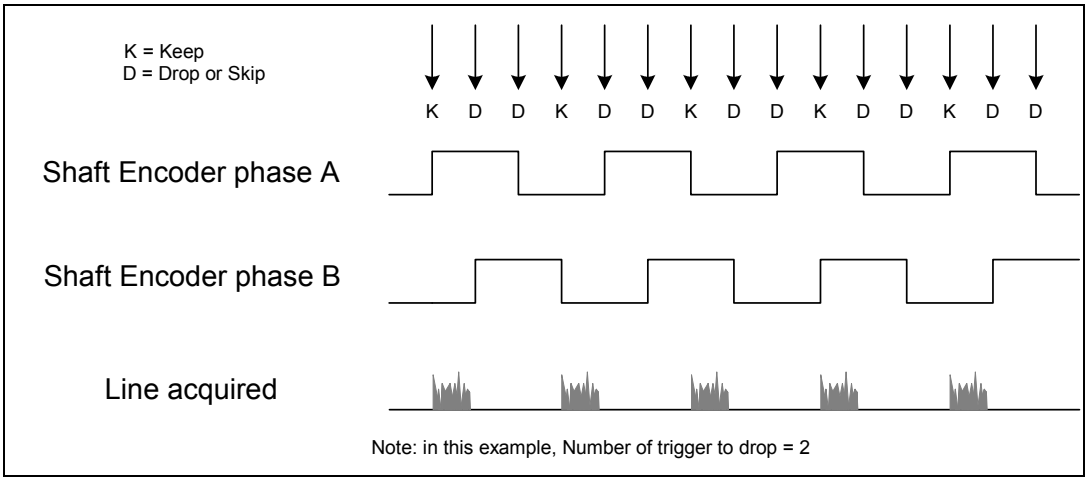

Figure 23: Encoder Input with Pulse-drop Counter

Example using Sequential Encoder Input

Support of a dual phase encoder should consider the direction of motion of one phase signal to the other. Such a case might exist where system vibrations and/or conveyor backlash can cause the encoder to briefly travel backwards. The acquisition device must in those cases count the reverse steps and subtract the forward steps such that only pulses after the reverse count reaches zero are considered. By using the event "Shaft Encoder Reverse Counter Overflow", an application can monitor an overflow of this counter. Also, if one wants to trigger a camera at its maximum line rate using a high jitter shaft encoder, the parameter CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY can be used to delay automatically line triggers to the camera to avoid over-triggering a camera, and thus not miss a line. Note that some cameras integrate this feature. See also the event "Line Trigger Too Fast" that can be enabled when using the 'auto delay' feature.

The example figure below shows shaft encoder signals with high jitter. If the acquisition is triggered when phase B follows phase A, with jitter present phase B may precede phase A. Use of the *Shaft Encoder Direction* parameter will prevent false trigger conditions.

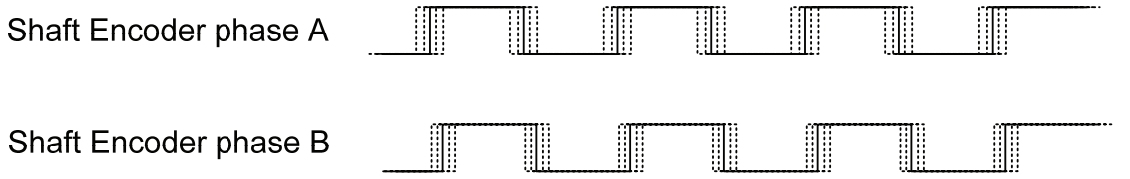

Figure 24: Using Shaft Encoder Direction Parameter

Note: Modify camera file parameters easily with the Sapera CamExpert program.

CVI/CCF File Parameters Used

Shaft Encoder Enable = X, where:

- If X = 1, Shaft Encoder is enabled
- If X = 0, Shaft Encoder is disabled

Shaft Encoder Pulse Drop = X, where:

- X = number of trigger pulses ignored between valid triggers

Shaft Encoder Pulse Multiply = X, where:

- X = number of trigger pulses generated for each shaft encoder pulses

Shaft Encoder Direction = X, where:

- X = 0, Ignore direction
- X = 1, Forward steps are detected by pulse order A/B (forward motion)
- X = 2, Forward steps are detected by pulse order B/A (reverse motion)

For information on camera configuration files, see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Virtual Frame Trigger for Line Scan Cameras

When using line scan cameras, a frame buffer is allocated in host system memory to store captured video lines. To control when a video line is stored as the first line in this "virtual" frame buffer, an external frame trigger signal is used. The Sapera vertical cropping parameter controls the number of lines sequentially grabbed and stored in the virtual frame buffer.

Virtual Frame Trigger Timing Diagram

The following timing diagram shows an example of grabbing 10 video lines from a line scan camera and the use of a virtual frame trigger to define when a video line is stored at the beginning of the virtual frame buffer. The virtual frame trigger signal (generated by some external event) connects to the X64 Xcelera-CL+ PX8 trigger input.

- Virtual frame trigger can be 24V industry standard, TTL 5V or RS-422 and be rising or falling edge active, active high or low, or double pulse rising or falling edge.
- In this example, virtual frame trigger control is configured for rising edge trigger.
- Virtual frame trigger connects to the X64 Xcelera-CL+ PX8 via the External Trigger Input 1 & 2 balanced inputs. Trigger Input 1 is available both on the board bracket J1 connector and from the internal J4 connector. Trigger input 2 is only on J4.
  - Trigger Input #1 on connector J1: pin 1 (+) and 9 (-)
  - Trigger Input #1 on connector J4: pin 19 (+) and pin 20 (-)
  - Trigger Input #2 on connector J4: pin 21 (+) and 22 (-) for input #2
- Two types of external connector brackets are available to bring out signals from the J4 connector.
- Camera control signals are active at all times. These continually trigger the camera acquisition in order to avoid corrupted video lines at the beginning of a virtual frame.
- The camera control signals are either timing controls on X64 Xcelera-CL+ PX8 shaft encoder inputs, or line triggers generated internally by the X64 Xcelera-CL+ PX8.
- The Sapera vertical cropping parameter specifies the number of lines captured.

Synchronization Signals for a 10 Line Virtual Frame

The following timing diagram shows the relationship between External Frame Trigger input, External Shaft Encoder input (one phase used with the second terminated), and camera control output to the camera.

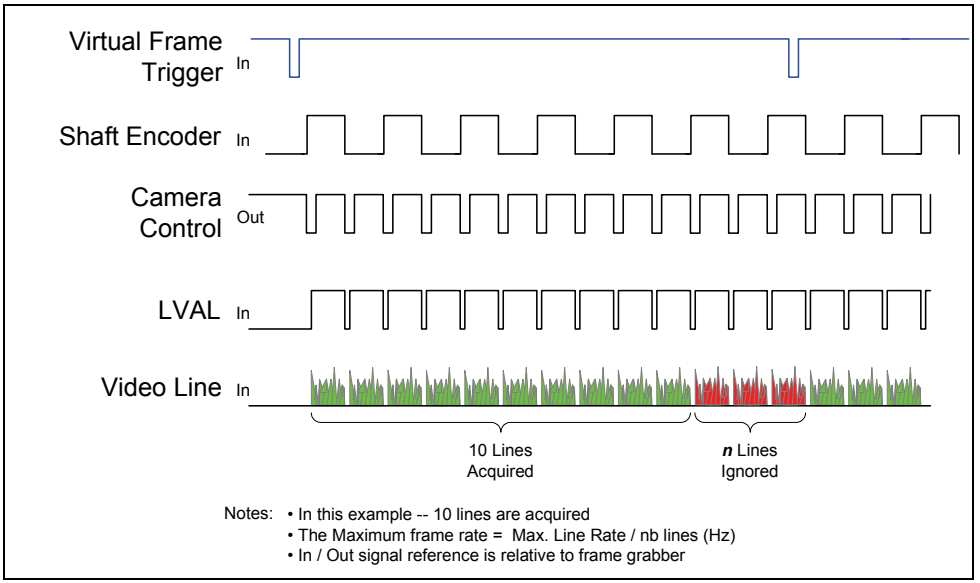

Figure 25: Synchronization Signals for a 10 Line Virtual Frame

CVI File (VIC) Parameters Used

The VIC parameters listed below provide the control functionality for virtual frame reset. Sapera applications load pre-configured CVI files or change VIC parameters during runtime.

Note that Sapera camera file parameters are easily modified by using the CamExpert program.

External Frame Trigger Enable = X, where: (with Virtual Frame Trigger enabled)

- If X = 1, External Frame Trigger is enabled
- If X = 0, External Frame Trigger is disabled

External Frame Trigger Detection = Y, where: (with Virtual Frame Trigger edge select)

- If Y= 1, External Frame Trigger is active low
- If Y= 2, External Frame Trigger is active high
- If Y= 4, External Frame Trigger is active on rising edge
- If Y= 8, External Frame Trigger is active on falling edge
- If Y= 32, External Frame Trigger is dual-input rising edge
- If Y= 64, External Frame Trigger is dual-input falling edge

External Frame Trigger Level = Z, where: (with Virtual Frame Trigger signal type)

- If Z= 2, External Frame Trigger is a RS-422 signal

For information on camera files, see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Sapera Acquisition Methods

Sapera acquisition methods define the control and timing of the camera and frame grabber board. Various methods are available, grouped as:

- Camera Trigger Methods (method 1 supported)
- Camera Reset Methods (method 1 supported)
- Line Integration Methods (method 1 through 4, 7 supported)
- Time Integration Methods (method 1 through 9 supported)
- Strobe Methods (method 1 through 4 supported)

Refer to the Sapera LT Acquisition Parameters Reference manual (OC-SAPM-APR00) for detailed information concerning camera and acquisition control methods.

Trigger to Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger-to-image reliability model brings together all the requirements for image acquisition to a central management unit. These include signals to control camera timing, on-board FIFO memory to compensate for PCI bus latency, and comprehensive error notification. If the X64 Xcelera-CL+ PX8 detects a problem, the application can take appropriate action to return to normal operation.

The X64 Xcelera-CL+ PX8 is designed with a robust ACU (Acquisition and Control Unit). The ACU monitors in real-time, the acquisition state of the input plus the DTE (Data Transfer Engine) which transfers image data from on-board memory into PC memory. In general, these management processes are transparent to end-user applications. With the X64 Xcelera-CL+ PX8, applications ensure trigger-to-image reliability by monitoring events and controlling transfer methods as described below:

Supported Events and Transfer Methods

Listed below are the supported acquisition and transfer events. Event monitoring is a major component to the Trigger-to-Image Reliability framework.

Acquisition Events

Acquisition events pertain to the acquisition module. They provide feedback on the image capture phase.

- **External Trigger** (Used/Ignored)
  Generated when the external trigger pin is asserted, which indicates the start of the acquisition process. There are two types of external trigger events: 'Used' or 'Ignored'. Following an external trigger, if the event generates a captured image, an External Trigger Used event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER).
  If there is no captured image, an External Trigger Ignored event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED). An external trigger event is ignored if the event rate is higher than the possible frame rate of the camera.
- **Start of Frame**
  Event generated during acquisition, with the detection of the start of a video frame by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_START_OF_FRAME.
- **End of Frame**
  Event generated during acquisition, with the detection of the end of a video frame by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_END_OF_FRAME.
- **Data Overflow**
  The Data Overflow event indicates that there is not enough bandwidth for the acquired data transfer without loss. Data Overflow would occur with limitations of the acquisition module and should never occur.
  The Sapera event value is CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW.
- **Frame Valid**
  Event generated on detection of the start of a video frame by the board acquisition hardware. Acquisition does not need to be active; therefore, this event can verify a valid signal is connected. The Sapera event value is CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC.
- **Pixel Clock** (Present/Absent)
  Event generated on the transition from detecting or not detecting a pixel clock signal. The Sapera event values are CORACQ_VAL_EVENT_TYPE_NO_PIXEL_CLK and CORACQ_VAL_EVENT_TYPE_PIXEL_CLK.
- **Frame Lost**
  The Frame Lost event indicates that an acquired image failed to transfer to on-board memory. An example is if there are no free on-board buffers available for the new image. This may be the case if the image transfer from onboard buffers to host PC memory is not sustainable due to bus bandwidth issues.
  The Sapera event value is CORACQ_VAL_EVENT_TYPE_FRAME_LOST.

- **Vertical Timeout**
  This event indicates a timeout situation where a camera fails to output a video frame after a trigger. The Sapera event value is CORACQ_VAL_EVENT_TYPE_VERTICAL_TIMEOUT.
- **External Line Trigger Too Slow**
  Event which indicates that the detected shaft encoder input tick rate is too slow for the device to take into account the specified shaft encoder multiplier value. The Sapera event value is CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW.
- **Line Trigger Too Fast**
  Event which indicates a previous line-trigger did not generate a complete video line from the camera. Note that due to jitter associated with using shaft encoders, the acquisition device can delay a line trigger if a previous line has not yet completed. This event is generated if a second line trigger comes in while the previous one is still pending. This event is generated once per virtual frame. The Sapera event value is CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST.
- **Shaft Encoder Reverse Count Overflow**
  Event which indicates that the shaft encoder has travelled in the opposite direction expected and that the number of pulses encountered during that travel has exceeded the acquisition device counter. The acquisition device will thus not be able to skip the appropriate number of pulses when the expected direction is detected. The Sapera event value is CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW

Transfer Events

Transfer events are the ones related to the transfer module. Transfer events provide feedback on image transfer from onboard memory frame buffers to PC memory frame buffers.

- **Start of Frame**
  Start of Frame event generated when the first image pixel is transferred from on-board memory into PC memory.
  The Sapera event value is CORXFER_VAL_EVENT_TYPE_START_OF_FRAME.
- **End of Frame**
  End of Frame event generated when the last image pixel is transferred from on-board memory into PC memory.
  The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_FRAME.
- **End of Line**
  End of Line event generated after a video line is transferred to a PC buffer.
  The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_LINE.
- **End of N Lines**
  End of N Lines event generated after a set number of video lines are transferred to a PC buffer.
  The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_NLINES.
- **End of Transfer**
  End of Transfer event generated at the completion of the last image transfer from on-board memory into PC memory. Issue a stop command to the transfer module to complete a transfer (if transfers are already in progress). If a frame transfer of a fixed number of images is requested, the transfer module will stop transfer automatically. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER.

Trigger Signal Validity

The ACU ignores external trigger signal noise with its programmable debounce control. Program the debounce parameter for the minimum pulse duration considered as a valid external trigger pulse. Refer to "Note 3: External Trigger Input Specifications" on page 105 for more information.

Supported Transfer Cycling Methods

The X64 Xcelera-CL+ PX8 supports the following transfer modes, which are either synchronous or asynchronous. These definitions are from the Sapera Basic Reference manual.

- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH
  Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the transfer will be done in the trash buffer, which is defined as the last buffer in the list; otherwise, it will occur in the next buffer. After a transfer to the trash buffer is done, the transfer device will check again the state of the next buffer. If it is empty, it will transfer to this buffer otherwise it will transfer again to the trash buffer.
- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH
  Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the next buffer will be skipped, and the transfer will be done in the trash buffer, which is defined as the last buffer in the list; otherwise it will occur in the next buffer. After a transfer to the trash is done, the transfer device will check the next buffer in the list, if its state is empty, it will transfer to this buffer otherwise it will skip it, and transfer again to the trash buffer.
- CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS
  The transfer device cycles through all buffers in the list without concern about the buffer state.

Output LUT Availability

The following table defines the supported output LUT (look up tables) for the X64 Xcelera-CL+ PX8. Note that unsupported modes are not listed.

Number of Digital Bits	Number of Taps Full	Number of Taps Medium	Number of Taps Dual Base	Output Pixel Format	LUT Format	Notes
8	8	4	3	MONO 8	8-in, 8-out	
8	8	4	3	MONO 16	8-in, 8-out	8 bits in 8 LSBs of 16-bit
8	10	-	-	MONO 8	8-in, 8-out	
10	8	2	2	MONO 8	10-in, 8-out	
10	8	2	2	MONO 16	10-in, 10-out	10 bits in 10 LSBs of 16-bit
12	4	2	2	MONO 8	12-in, 8-out	8 MSB
12	4	2	2	MONO 16	12-in, 12-out	12 bits in 12 LSBs of 16-bit
8 x 3 (RGB)	2	1	1	RGB8888	8-in, 8-out	
10 x 3 (RGB)	1	1	-	RGB8888 RGB101010 RGB16161616	10-in, 8-out 10-in, 10-out 10-in, 10-out	Medium or Full
12 x 3 (RGB)	1	1	-	RGB8888 RGB101010 RGB16161616	12-in, 8-out 12-in, 10-out 12-in, 12-out	Medium or Full

Table 9: Output LUT Availability

Supporting Non-Standard Camera Link Cameras

High performance cameras that output 10 taps/8-bits or 8 taps/10-bits cannot interface with a standard Camera Link full specification frame grabber. The X64 Xcelera-CL+ PX8 Full provides support for those non-standard formats by using specific firmware easily uploaded when required. Described below is this format along with an example camera that uses this non-standard format.

Firmware: 10 Taps Camera @ 8 bits

- Supports 10 taps @ 8 bits cameras only such as Basler A504K
- This Camera Link utilization is not compatible with the standard 8 tap full specification
- Output LUT and Flat Field Correction are available
- The following table describes the Bit assignment
- Tap 1 Bits are D0_x … Tap 10 Bits are D9_x

Connector 1: Channel Link No. X		**Connector 2: Channel Link No. Y**		**Connector 2: Channel Link No. Z**	
Bit Name	Camera / Frame Grabber Pin	Bit Name	Camera / Frame Grabber Pin	Bit Name	Camera / Frame Grabber Pin
D0_0	Tx0/Rx0	D3_2	Tx0/Rx0	D6_5	Tx0/Rx0
D0_1	Tx1/Rx1	D3_3	Tx1/Rx1	D6_6	Tx1/Rx1
D0_2	Tx2/Rx2	D3_4	Tx2/Rx2	D6_7	Tx2/Rx2
D0_3	Tx3/Rx3	D3_5	Tx3/Rx3	D7_0	Tx3/Rx3
D0_4	Tx4/Rx4	D3_6	Tx4/Rx4	D7_1	Tx4/Rx4
D0_5	Tx5/Rx5	D3_7	Tx5/Rx5	D7_2	Tx5/Rx5
D0_6	Tx6/Rx6	D4_0	Tx6/Rx6	D7_3	Tx6/Rx6
D0_7	Tx7/Rx7	D4_1	Tx7/Rx7	D7_4	Tx7/Rx7
D1_0	Tx8/Rx8	D4_2	Tx8/Rx8	D7_5	Tx8/Rx8
D1_1	Tx9/Rx9	D4_3	Tx9/Rx9	D7_6	Tx9/Rx9
D1_2	Tx10/Rx10	D4_4	Tx10/Rx10	D7_7	Tx10/Rx10
D1_3	Tx11/Rx11	D4_5	Tx11/Rx11	D8_0	Tx11/Rx11
D1_4	Tx12/Rx12	D4_6	Tx12/Rx12	D8_1	Tx12/Rx12
D1_5	Tx13/Rx13	D4_7	Tx13/Rx13	D8_2	Tx13/Rx13
D1_6	Tx14/Rx14	D5_0	Tx14/Rx14	D8_3	Tx14/Rx14
D1_7	Tx15/Rx15	D5_1	Tx15/Rx15	D8_4	Tx15/Rx15
D2_0	Tx16/Rx16	D5_2	Tx16/Rx16	D8_5	Tx16/Rx16

D2_1	Tx17/Rx17	D5_3	Tx17/Rx17	D8_6	Tx17/Rx17
D2_2	Tx18/Rx18	D5_4	Tx18/Rx18	D8_7	Tx18/Rx18
D2_3	Tx19/Rx19	D5_5	Tx19/Rx19	D9_0	Tx19/Rx19
D2_4	Tx20/Rx20	D5_6	Tx20/Rx20	D9_1	Tx20/Rx20
D2_5	Tx21/Rx21	D5_7	Tx21/Rx21	D9_2	Tx21/Rx21
D2_6	Tx22/Rx22	D6_0	Tx22/Rx22	D9_3	Tx22/Rx22
D2_7	Tx23/Rx23	D6_1	Tx23/Rx23	D9_4	Tx23/Rx23
LVAL	Tx24/Rx24	D6_2	Tx24/Rx24	D9_5	Tx24/Rx24
FVAL	Tx25/Rx25	D6_3	Tx25/Rx25	D9_6	Tx25/Rx25
D3_0	Tx26/Rx26	D6_4	Tx26/Rx26	D9_7	Tx26/Rx26
D3_1	Tx27/Rx27	LVAL	Tx27/Rx27	LVAL	Tx27/Rx27

Table 10: 10 Taps Camera @ 8 bits Pinout

Firmware: 8-Taps @ 10-bits Camera Link

- Supports 8 taps @ 10-bits cameras only such as Basler A406K
- This Camera Link utilization is not compatible with the standard 8 tap full specification
- Output LUT and Flat Field Correction are available
- The following table describes the Bit assignment
- Tap 1 Bits are D0_x … Tap 8 Bits are D7_x

Connector 1: Channel Link No. X		**Connector 2: Channel Link No. Y**		**Connector 2: Channel Link No. Z**	
Bit Name	Camera / Frame Grabber Pin	Bit Name	Camera / Frame Grabber Pin	Bit Name	Camera / Frame Grabber Pin
D0_2	Tx0/Rx0	D3_2	Tx0/Rx0	D6_2	Tx0/Rx0
D0_3	Tx1/Rx1	D3_3	Tx1/Rx1	D6_3	Tx1/Rx1
D0_4	Tx2/Rx2	D3_4	Tx2/Rx2	D6_4	Tx2/Rx2
D0_5	Tx3/Rx3	D3_5	Tx3/Rx3	D6_5	Tx3/Rx3
D0_6	Tx4/Rx4	D3_6	Tx4/Rx4	D6_6	Tx4/Rx4
D0_7	Tx5/Rx5	D3_7	Tx5/Rx5	D6_7	Tx5/Rx5
D0_8	Tx6/Rx6	D3_8	Tx6/Rx6	D6_8	Tx6/Rx6
D0_9	Tx7/Rx7	D3_9	Tx7/Rx7	D6_9	Tx7/Rx7
D1_2	Tx8/Rx8	D4_2	Tx8/Rx8	D7_2	Tx8/Rx8
D1_3	Tx9/Rx9	D4_3	Tx9/Rx9	D7_3	Tx9/Rx9

D1_4	Tx10/Rx10	D4_4	Tx10/Rx10	D7_4	Tx10/Rx10
D1_5	Tx11/Rx11	D4_5	Tx11/Rx11	D7_5	Tx11/Rx11
D1_6	Tx12/Rx12	D4_6	Tx12/Rx12	D7_6	Tx12/Rx12
D1_7	Tx13/Rx13	D4_7	Tx13/Rx13	D7_7	Tx13/Rx13
D1_8	Tx14/Rx14	D4_8	Tx14/Rx14	D7_8	Tx14/Rx14
D1_9	Tx15/Rx15	D4_9	Tx15/Rx15	D7_9	Tx15/Rx15
D2_2	Tx16/Rx16	D5_2	Tx16/Rx16	D2_1	Tx16/Rx16
D2_3	Tx17/Rx17	D5_3	Tx17/Rx17	D3_0	Tx17/Rx17
D2_4	Tx18/Rx18	D5_4	Tx18/Rx18	D3_1	Tx18/Rx18
D2_5	Tx19/Rx19	D5_5	Tx19/Rx19	D4_0	Tx19/Rx19
D2_6	Tx20/Rx20	D5_6	Tx20/Rx20	D4_1	Tx20/Rx20
D2_7	Tx21/Rx21	D5_7	Tx21/Rx21	D5_0	Tx21/Rx21
D2_8	Tx22/Rx22	D5_8	Tx22/Rx22	D5_1	Tx22/Rx22
D2_9	Tx23/Rx23	D5_9	Tx23/Rx23	D6_0	Tx23/Rx23
LVAL	Tx24/Rx24	LVAL	Tx24/Rx24	LVAL	Tx24/Rx24
FVAL	Tx25/Rx25	D1_0	Tx25/Rx25	D6_1	Tx25/Rx25
D0_0	Tx26/Rx26	D1_1	Tx26/Rx26	D7_0	Tx26/Rx26
D0_1	Tx27/Rx27	D2_0	Tx27/Rx27	D7_1	Tx27/Rx27

Table 11: 8 Taps Camera @ 10- bits Pinout

X64 Xcelera-CL+ PX8 Supported Parameters

The tables below describe the Sapera capabilities supported by the X64 Xcelera-CL+ PX8. Unless specified, each capability applies to both boards or all mode configurations and all acquisition modes.

The information here is subject to change. The application needs to verify capabilities. New board driver releases may change product specifications.

Sapera describes the X64 Xcelera-CL+ PX8 family as:

- Board Server: Xcelera-CL_PX8_1
- Acquisition Module: *dependent on firmware used*

Camera Related Capabilities

Capability	Values
CORACQ_CAP_CONNECTOR_TYPE	CORACQ_VAL_CONNECTOR_TYPE_CAMLINK (0x2)
CORACQ_CAP_CONNECTOR_CAMLINK (Pin – 01, Pin – 02, Pin – 03)	CORACQ_VAL_SIGNAL_NAME_NO_CONNECT (0x1) CORACQ_VAL_SIGNAL_NAME_PULSE0 (0x8) CORACQ_VAL_SIGNAL_NAME_PULSE1 (0x10) CORACQ_VAL_SIGNAL_NAME_GND (0x4000)
CORACQ_CAP_CONNECTOR_CAMLINK (Pin – 04)	CORACQ_VAL_SIGNAL_NAME_NO_CONNECT (0x1)

Table 12: Camera Related Capabilities

Camera Related Parameters

Parameter		Values
CORACQ_PRM_CHANNEL	*Medium/Full Mono*	CORACQ_VAL_CHANNEL_SINGLE (0x1) CORACQ_VAL_CHANNEL_DUAL (0x2)
	Base/Medium RGB *Bayer/ 10-taps/8T10B*	CORACQ_VAL_CHANNEL_SINGLE (0x1)
CORACQ_PRM_FRAME		CORACQ_VAL_FRAME_PROGRESSIVE (0x2)
CORACQ_PRM_INTERFACE		CORACQ_VAL_INTERFACE_DIGITAL (0x2)
CORACQ_PRM_SCAN		CORACQ_VAL_SCAN_AREA (0x1) CORACQ_VAL_SCAN_LINE (0x2)
CORACQ_PRM_SIGNAL		CORACQ_VAL_SIGNAL_DIFFERENTIAL (0x2)
CORACQ_PRM_VIDEO	*Mono/Bayercolor RGB*	CORACQ_VAL_VIDEO_MONO (0x1) CORACQ_VAL_VIDEO_RGB (0x8)
CORACQ_PRM_PIXEL_DEPTH	*mono*	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO10 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO12 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 14 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO14 16 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16
	color RGB	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI12
	Bayer	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 12 bits, # LUT = 0, LUT format = CORDATA_FORMAT_COLORNI10
	10-taps	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8
	8T10B	10 bits, # LUT = 1, LUT format = CORDATA_FORMATMONO10
CORACQ_PRM_VIDEO_STD		CORACQ_VAL_VIDEO_STD_NON_STD (0x1)
CORACQ_PRM_FIELD_ORDER		CORACQ_VAL_FIELD_ORDER_NEXT_FIELD (0x4)

CORACQ_PRM_HACTIVE	mono/color RGB	min = 1 pixel max = 16777215 pixel step = 1 pixel
	Bayer	min = 1 pixel max = 8192 pixel step = 1 pixel
CORACQ_PRM_HSYNC		min = 4 pixel max = 4294967295 pixel step = 1 pixel
CORACQ_PRM_VACTIVE		min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_VSYNC		min = 0 line max = 4294967295 line step = 1 line
CORACQ_PRM_HFRONT_INVALID		min = 0 pixel max = 16777215 pixel step = 1 pixel
CORACQ_PRM_HBACK_INVALID		min = 0 pixel max = 16777215 pixel step = 1 pixel
CORACQ_PRM_VFRONT_INVALID		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_VBACK_INVALID		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_PIXEL_CLK_SRC		CORACQ_VAL_PIXEL_CLK_SRC_EXT (0x2)
CORACQ_PRM_PIXEL_CLK_EXT		min = 20000000 Hz max = 85000000 Hz step = 1 Hz
CORACQ_PRM_SYNC		CORACQ_VAL_SYNC_SEP_SYNC (0x4)
CORACQ_PRM_HSYNC_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1)
CORACQ_PRM_VSYNC_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1)
CORACQ_PRM_TIME_INTEGRATE_METHOD		CORACQ_VAL_TIME_INTEGRATE_METHOD_1 (0x1) CORACQ_VAL_TIME_INTEGRATE_METHOD_2 (0x2) CORACQ_VAL_TIME_INTEGRATE_METHOD_3 (0x4) CORACQ_VAL_TIME_INTEGRATE_METHOD_4 (0x8) CORACQ_VAL_TIME_INTEGRATE_METHOD_5 (0x10) CORACQ_VAL_TIME_INTEGRATE_METHOD_6 (0x20) CORACQ_VAL_TIME_INTEGRATE_METHOD_7 (0x40) CORACQ_VAL_TIME_INTEGRATE_METHOD_8 (0x80) CORACQ_VAL_TIME_INTEGRATE_METHOD_9 (0x100)
CORACQ_PRM_CAM_TRIGGER_METHOD		CORACQ_VAL_CAM_TRIGGER_METHOD_1 (0x1) CORACQ_VAL_CAM_TRIGGER_METHOD_2 (0x2)
CORACQ_PRM_CAM_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_CAM_TRIGGER_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_RESET_METHOD		CORACQ_VAL_CAM_RESET_METHOD_1 (0x1)
CORACQ_PRM_CAM_RESET_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)

CORACQ_PRM_CAM_RESET_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_NAME	mono color RGB Bayer	Default Area Scan 1 tap Mono Default Area Scan 1 tap Color Default Bayer Area Scan 1 tap Color
	10-taps	Default Area Scan 10 taps Parallel Mono
	8T10B	Default Area Scan 8 taps Parallel Mono
CORACQ_PRM_LINE_INTEGRATE_METHOD		CORACQ_VAL_LINE_INTEGRATE_METHOD_1 (0x1) CORACQ_VAL_LINE_INTEGRATE_METHOD_2 (0x2) CORACQ_VAL_LINE_INTEGRATE_METHOD_3 (0x4) CORACQ_VAL_LINE_INTEGRATE_METHOD_4 (0x8) CORACQ_VAL_LINE_INTEGRATE_METHOD_7 (0x40)
CORACQ_PRM_LINE_TRIGGER_METHOD		CORACQ_VAL_LINE_TRIGGER_METHOD_1 (0x1)
CORACQ_PRM_LINE_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_TRIGGER_DELAY		min = 0 µs max = 65535 µs step = 1 µs
CORACQ_PRM_LINE_TRIGGER_DURATION		min = 0 µs max = 65535 µs step = 1 µs
CORACQ_PRM_TAPS	*Full mono/ Full Bayer* *color RGB* *Base Bayer/Medium RGB*	min = 1 tap, max = 8 taps, step = 1 tap min = 1 tap, max = 4 taps, step = 1 tap min = 1 tap, max = 3 taps, step = 1 tap
	10-taps	min = 10 taps, max = 10 taps, step = 1 tap
	8T10B	min = 8 taps, max = 8 taps, step = 1 tap
CORACQ_PRM_TAP_OUTPUT	Medium/Full mono / Bayer	CORACQ_VAL_TAP_OUTPUT_ALTERNATE (0x1) CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2) CORACQ_VAL_TAP_OUTPUT_PARALLEL (0x4)
	color RGB	CORACQ_VAL_TAP_OUTPUT_ALTERNATE (0x1) CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2)
	10-taps / 8T10B	CORACQ_VAL_TAP_OUTPUT_PARALLEL (0x4)
CORACQ_PRM_TAP_1_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_2_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_3_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)

CORACQ_PRM_TAP_4_DIRECTION	Full mono/medium color RGB only	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_5_DIRECTION	*Full mono only*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_6_DIRECTION	*Full mono only*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_7_DIRECTION	*Full mono only*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_8_DIRECTION	*Full mono only*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_PIXEL_CLK_DETECTION		CORACQ_VAL_RISING_EDGE (0x4)
CORACQ_PRM_CHANNELS_ORDER		CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x1) CORACQ_VAL_CHANNELS_ORDER_REVERSE (0x2)
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN		1 Hz
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX		16777215 Hz
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MIN		1 µs
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MAX		65535000 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DELAY		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DURATION		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_IO_CONTROL (*)		
CORACQ_PRM_TIME_INTEGRATE_PULSE0_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_PULSE0_DELAY		min = 0 µs max = 65535000 µs step = 1 µs

CORACQ_PRM_TIME_INTEGRATE_PULSE0_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE1_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_INTEGRATE_PULSE1_DELAY		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE1_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE0_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_INTEGRATE_PULSE0_DELAY		min = 0 µs max = 65535 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE0_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAMLINK_CONFIGURATION	Full Mono/Full Bayer	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1) CORACQ_VAL_CAMLINK_CONFIGURATION_MEDIUM (0x2) CORACQ_VAL_CAMLINK_CONFIGURATION_FULL (0x4) CORACQ_VAL_CAMLINK_CONFIGURATION_2BASE (0x8)
	Medium Mono	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1) CORACQ_VAL_CAMLINK_CONFIGURATION_MEDIUM (0x2) CORACQ_VAL_CAMLINK_CONFIGURATION_2BASE (0x8)
	medium color RGB/medium Bayer	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1) CORACQ_VAL_CAMLINK_CONFIGURATION_MEDIUM (0x2)
	Base Bayer	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1)
	10-taps	CORACQ_VAL_CAMLINK_CONFIGURATION_10TAPS_FORMAT2 (0x40)
CORACQ_PRM_DATA_VALID_ENABLE	Mono	TRUE FALSE
	10 taps / 8T10B	Not available
CORACQ_PRM_DATA_VALID_POLARITY		CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TAP_9_DIRECTION	*10-taps only*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_10_DIRECTION	*10-taps only*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TIMESLOT	10-taps / 8T10B only	CORACQ_VAL_TIMESLOT_1 (0x1)
	Others	CORACQ_VAL_TIMESLOT_1 (0x1) CORACQ_VAL_TIMESLOT_2 (0x2)

CORACQ_PRM_BAYER_ALIGNMENT	mono, color RGB	Not available
	Bayer	CORACQ_VAL_BAYER_ALIGNMENT_GB_RG (0x1) CORACQ_VAL_BAYER_ALIGNMENT_BG_GR (0x2) CORACQ_VAL_BAYER_ALIGNMENT_RG_GB (0x4) CORACQ_VAL_BAYER_ALIGNMENT_GR_BG (0x8)
CORACQ_PRM_CAM_CONTROL_DURING_READOUT		TRUE FALSE
CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY		CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_DISABLE CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_FREQ_MAX

Table 13: Camera Related Parameters

VIC Related Parameters

Parameter		Values
CORACQ_PRM_CAMSEL	Mono/Bayer	CAMSEL_MONO = from 0 to 0
	color RGB	CAMSEL_RGB = from 0 to 0
CORACQ_PRM_CROP_LEFT		min = 0 pixel max = 16777215 pixel step = 16 pixel
CORACQ_PRM_CROP_TOP		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_CROP_WIDTH		min = 16 pixel max = 16777215 pixel step = 16 pixel
CORACQ_PRM_CROP_HEIGHT		min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_DECIMATE_METHOD		CORACQ_VAL_DECIMATE_DISABLE (0x1)
CORACQ_PRM_LUT_ENABLE		TRUE FALSE
CORACQ_PRM_LUT_NUMBER		Default = 0
CORACQ_PRM_STROBE_ENABLE		TRUE FALSE
CORACQ_PRM_STROBE_METHOD		CORACQ_VAL_STROBE_METHOD_1 (0x1) CORACQ_VAL_STROBE_METHOD_2 (0x2) CORACQ_VAL_STROBE_METHOD_3 (0x4) CORACQ_VAL_STROBE_METHOD_4 (0x8)
CORACQ_PRM_STROBE_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_STROBE_DURATION		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_STROBE_DELAY		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_ENABLE		TRUE FALSE

CORACQ_PRM_TIME_INTEGRATE_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_CAM_RESET_ENABLE		TRUE FALSE
CORACQ_PRM_OUTPUT_FORMAT	*mono*	CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16
	color RGB	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_RGB16161616
	Bayer	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16
CORACQ_PRM_EXT_TRIGGER_ENABLE		CORACQ_VAL_EXT_TRIGGER_OFF (0x1) CORACQ_VAL_EXT_TRIGGER_ON (0x8)
CORACQ_PRM_VIC_NAME	Mono	Default Area Scan 1 tap Mono
	Color RGB	Default Area Scan 1 tap Color
	Bayer	Default Bayer Area Scan 1 tap Color
	10-taps	Default Area Scan 10 taps Parallel Mono
	8T10B	Default Area Scan 8 taps Parallel Mono
CORACQ_PRM_LUT_MAX		1
CORACQ_PRM_EXT_TRIGGER_DETECTION		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_LUT_FORMAT	*mono*	Default = CORACQ_VAL_OUTPUT_FORMAT_MONO8
	color RGB	Default = CORACQ_VAL_OUTPUT_FORMAT_RGB16161616
	bayer	Default = CORACQ_VAL_OUTPUT_FORMAT_MONO16
CORACQ_PRM_VSYNC_REF		CORACQ_VAL_SYNC_REF_END (0x2)
CORACQ_PRM_HSYNC_REF		CORACQ_VAL_SYNC_REF_END (0x2)
CORACQ_PRM_LINE_INTEGRATE_ENABLE		TRUE FALSE
CORACQ_PRM_LINE_INTEGRATE_DURATION		min = 1 pixel max = 16777215 pixel step = 1 pixel
CORACQ_PRM_LINE_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_DETECTION		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8) CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE (0x20) CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE (0x40)
CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION		CORACQ_VAL_RISING_EDGE (0x4)

CORACQ_PRM_SNAP_COUNT	min = 1 frame max = 65535 frame step = 1 frame
CORACQ_PRM_INT_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_LINE_TRIGGER_FREQ	Default = 5000 Hz
CORACQ_PRM_BIT_ORDERING	CORACQ_VAL_BIT_ORDERING_STD (0x1)
CORACQ_PRM_EXT_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_STROBE_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1)
CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MIN	245 Hz
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MAX	500000 Hz
CORACQ_PRM_MASTER_MODE	Not available
CORACQ_PRM_SHAFT_ENCODER_DROP	min = 0 tick max = 255 tick step = 1 tick
CORACQ_PRM_SHAFT_ENCODER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	min = 1 frame max = 65534 frame step = 1 frame
CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	min = 1 milli-Hz max = 1073741823 milli-Hz step = 1 milli-Hz
CORACQ_PRM_STROBE_DELAY_2	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_FRAME_LENGTH	CORACQ_VAL_FRAME_LENGTH_FIX (0x1) CORACQ_VAL_FRAME_LENGTH_VARIABLE (0x2)
CORACQ_PRM_FLIP mono	CORACQ_VAL_FLIP_OFF (0x00) CORACQ_VAL_FLIP_HORZ (0x01)
10 taps / 8T10B/Bayer	Not Available
CORACQ_PRM_EXT_TRIGGER_DURATION	min = 0 µs max = 255 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_RESET_DELAY	min = 0 µs max = 0 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_SHAFT_ENCODER_LEVEL	CORACQ_VAL_LEVEL_422 (0x2)

CORACQ_PRM_EXT_FRAME_TRIGGER_SOURCE (*)		min = 0 max = 5 step = 1
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE (*)		min = 0 max = 7 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE (*)		min = 0 max = 5 step = 1
CORACQ_PRM_SHAFT_ENCODER_MULTIPLY		min = 1 max = 32 step = (2**N)
CORACQ_PRM_PLANAR_INPUT_SOURCES		Not available
CORACQ_PRM_EXT_TRIGGER_DELAY		min = 0 max = 65535000 step = 1
CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE		CORACQ_VAL_TIME_BASE_US (0x1) CORACQ_VAL_TIME_BASE_LINE (0x4) CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0x8)
CORACQ_PRM_BAYER_DECODER_ENABLE	Full	Not available (mono or color RGB)
	Bayer	TRUE / FALSE
CORACQ_PRM_BAYER_DECODER_METHOD	Full	Not available (mono or color RGB)
	Bayer	CORACQ_VAL_BAYER_DECODER_METHOD_1 (0x1)
CORACQ_PRM_BAYER_DECODER_WB_GAIN	Full	Not available (mono or color RGB)
	Bayer	min = 100000 max = 899609 step = 1
CORACQ_PRM_BAYER_DECODER_WB_GAIN_RED	Full	Not available (mono or color RGB)
	Bayer	min = 100000 max = 499609 step = 1
CORACQ_PRM_BAYER_DECODER_WB_GAIN_GREEN	Full	Not available (mono or color RGB)
	Bayer	min = 100000 max = 499609 step = 1
CORACQ_PRM_BAYER_DECODER_WB_GAIN_BLUE	Full	Not available (mono or color RGB)
	Bayer	min = 100000 max = 899609 step = 1
CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY		min = 0 max = 65535000 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE_STR		[0] = Automatic [1] = From External Trigger #1 [2] = From External Trigger #2 [3] = From Board Sync [4] = To Board Sync [5] = Pulse to Board Sync

CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE_STR		[0] = Automatic [1] = From Shaft Encoder Phase A [2] = From Shaft Encoder Phase B [3] = From Shaft Encoder Phase A & B [4] = From Board Sync [5] = To Board Sync [6] = Pulse to Board Sync [7] = To Board Sync When Grabbing
CORACQ_PRM_VERTICAL_TIMEOUT_DELAY		min = 0 max = 16383000 step = 1
CORACQ_PRM_BAYER_DECODER_SATURATION_FACTOR	Bayer	min = 0 max = 65535 step = 1
CORACQ_PRM_BAYER_DECODER_SATURATION_WEIGHT_RED	Bayer	min = 0 max = 65535 step = 1
CORACQ_PRM_BAYER_DECODER_SATURATION_WEIGHT_GREEN	Bayer	min = 0 max = 65535 step = 1
CORACQ_PRM_BAYER_DECODER_SATURATION_WEIGHT_BLUE	Bayer	min = 0 max = 65535 step = 1
CORACQ_PRM_POCL_ENABLE		TRUE FALSE
CORACQ_PRM_SHAFT_ENCODER_SOURCE (*)		min = 0 max = 2 step = 1
CORACQ_PRM_SHAFT_ENCODER_SOURCE_STR		[0] = Automatic [1] = From Shaft Encoder Opto-coupled [2] = From Shaft Encoder RS422
CORACQ_PRM_SHAFT_ENCODER_DIRECTION		CORACQ_VAL_SHAFT_ENCODER_DIRECTION_IGNORE (0x00) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_FORWARD (0x01) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_REVERSE (0x02)

Table 14: VIC Related Parameters

ACQ Related Parameters

Parameter		Values
CORACQ_PRM_LABEL	Full mono Medium mono color RGB 8T10B Full/Medium Bayer 10 taps	Camera Link Full Mono #1 Camera Link Medium Mono #1 Camera Link Medium Color RGB #1 Camera Link 8 Taps Parallel 10 Bits Mono #1 Camera Link Bayer #1 Camera Link 10 Taps Parallel Mono #1
	Dual mono	Camera Link Base Mono #1 Camera Link Base Mono #2
	Dual Bayer	Camera Link Bayer #1 Camera Link Bayer #2
CORACQ_PRM_EVENT_TYPE		CORACQ_VAL_EVENT_TYPE_START_OF_FRAME CORACQ_VAL_EVENT_TYPE_END_OF_FRAME CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC CORACQ_VAL_EVENT_TYPE_NO_PIXEL_CLK CORACQ_VAL_EVENT_TYPE_PIXEL_CLK CORACQ_VAL_EVENT_TYPE_FRAME_LOST CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED CORACQ_VAL_EVENT_TYPE_VERTICAL_TIMEOUT CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW
CORACQ_PRM_SIGNAL_STATUS		CORACQ_VAL_SIGNAL_HSYNC_PRESENT CORACQ_VAL_SIGNAL_VSYNC_PRESENT CORACQ_VAL_SIGNAL_PIXEL_CLK_PRESENT
CORACQ_PRM_FLAT_FIELD_SELECT		0
CORACQ_PRM_FLAT_FIELD_ENABLE	Medium/Full Mono/10 taps/8T10B	TRUE FALSE
	color RGB/Bayer	Not Available
CORACQ_CAP_FLAT_FIELD_OFFSET		min = 0 max = 255 step = 1
CORACQ_CAP_FLAT_FIELD_GAIN		min = 1 max = 255 step = 1
CORACQ_CAP_FLAT_FIELD_GAIN_DIVISOR		0x80
CORACQ_CAP_FLAT_FIELD_PIXEL_REPLACEMENT		TRUE: *Pixel replacement is usually done by averaging the 2 neighborhood pixels. When one of the neighbors is not available (border image pixels, and border internal packet pixels), the pixel is simply replaced with the available neighbor.
CORACQ_CAP_SERIAL_PORT_INDEX		Supported

Table 15: Acquisition Related Parameters

Windows Embedded 7 Installation

Windows Embedded 7 is not officially supported by Teledyne DALSA due to the number of possible configurations. However, Sapera LT and other Teledyne DALSA products should function properly on the Windows Embedded 7 platform provided that the required components are installed.

Teledyne DALSA provides answer files (.xml) for use during Windows Embedded 7 installation that install all necessary components for running Sapera LT 32-bit or 64-bit versions (SDK or Runtime), Sapera Processing 32-bit or 64-bit versions (SDK or Runtime), and Teledyne DALSA framegrabbers.

For each platform (32 or 64-bit), the answer file provided is:

- **SaperaFrameGrabbers.xml**:
  Configuration for Sapera LT, Sapera Processing and Teledyne DALSA framegrabbers

The file is located in the following directory dependent on the platform used:

```
<Install Directory>\Sapera\Install\Win7_Embedded\Win32
<Install Directory>\Sapera\Install\Win7_Embedded\Win64
```

The OS footprint for these configurations is less than 1 GB. Alternatively, the Windows Thin Client configuration template provided by Microsoft in the Windows Embedded 7 installation also provides the necessary dependencies for Sapera LT, and Teledyne DALSA framegrabbers (with an OS footprint of approximately 1.5 GB).

If you are installing other applications on the Windows Embedded 7 platform, it is recommended that you verify which components are required, and if necessary, create a corresponding “Answer File”.

For more information on performing dependency analysis to enable your application on Windows Embedded 7, refer to the Microsoft Windows Embedded 7 documentation.

Sapera Servers & Resources

Servers and Resources

The following table describes the X64 Xcelera-CL+ PX8 Full board

Servers	Resources			
Name	**Type**	**Name**	**Index**	**Description**
Xcelera-CL_PX8_1 (default firmware)	Acquisition	Camera Link Full Mono	0	Full configuration, monochrome output, Camera #1
		Camera Link Full Color RGB #1	1	Full configuration, RGB output, Camera #1
Xcelera-CL_PX8_1 (10 taps firmware)	Acquisition	Camera Link 10 Taps Parallel Mono #1	0	Full configuration, 10 Taps @ 8 bits, Camera #1
Xcelera-CL_PX8_1 (8 taps/10 bits firmware)	Acquisition	Camera Link 8 Taps Parallel 10 Bits Mono #1	0	Full configuration, 8 Taps @ 10 bits, Camera #1
Xcelera-CL_PX8_1 (Bayer firmware)	Acquisition	Camera Link Bayer #1	0	Base or Medium configuration, Bayer Decoder, Camera #1

Table 16: X64 Xcelera-CL+ PX8 Full Board - Servers and Resources

The following table describes the X64 Xcelera-CL+ PX8 Dual board

Servers		Resources		
Name	**Type**	**Name**	**Index**	**Description**
Xcelera-CL_PX8_1 (default Base firmware with FFC)	Acquisition	Camera Link Base Mono 1	0	Base configuration, monochrome Camera #1
		Camera Link Base Mono 2	1	Base configuration, monochrome Camera #2
		Camera Link Base RGB 1	2	Base configuration, color RGB Camera #1
		Camera Link Base RGB 2	3	Base configuration, color RGB Camera #2
Xcelera-CL_PX8_1 (Medium firmware with FFC)	Acquisition	Camera Link Medium Monochrome 1	0	Medium configuration, monochrome Camera #1
		Camera Link Medium Color RGB 1	1	Medium configuration, RGB Camera #1
Xcelera-CL_PX8_1 (Bayer Base firmware)	Acquisition	Camera Link Base Bayer 1	0	Base configuration, Bayer Decoder, Camera #1
		Camera Link Base Bayer 2	1	Base configuration Bayer Decoder, Camera #2
Xcelera-CL_PX8_1 (Bayer Medium firmware)		Camera Link Medium Bayer 1	0	Medium configuration, Bayer Decoder, Camera #1

Table 17: X64 Xcelera-CL+ PX8 Dual Board - Servers and Resources

Technical Specifications

X64 Xcelera-CL+ PX8 Board Specifications

Digital Video Input & Controls

Input Type	Camera Link Specifications Rev 1.2 compliant; 1Full or 1 Medium or 2 Base (using SDR-26 Camera Link connectors — MiniCL) Supports PoCL cameras
Common Pixel Formats	Camera Link tap configuration for 8, 10, 12, 14 and 16-bit mono, 24-bit RGB and Bayer, 30-bit RGB, 36-bit RGB
Tap Format Details	1 Tap – 8/10/12/14/16-bit mono 2 Taps – 8/10/12/14/16-bit mono 4 Taps – 8/10/12-bit mono 4 Taps – 14/16-bit mono (non-standard) 8 Taps – 8-bit mono 8 Taps – 10-bit mono (non-standard) 10 Taps – 8-bit mono (non-standard) 3 Taps – 8/10/12-bit RGB
Scanning	Area scan and Line scan: Progressive, Multi-Tap, Multi-Channel, Tap reversal, Segmented Tap Configuration, Alternate Tap Configuration
Scanning Directions	Left to Right, Right to Left, Up-Down, Down-Up From Top, From Middle, From Bottom
Resolution *note: these are X64 Xcelera-CL+ PX8 maximums, not Camera Link specifications*	Horizontal Minimum: 8 Pixels per tap (8-bits/pixel) Horizontal Maximum: 8-bits/pixel x 16 Million Pixels/line 16-bits/pixel x 8 Million Pixels/line 32-bits/pixel x 4 Million Pixels/line 64-bits/pixel x 2 Million Pixels/line Vertical Minimum: 1 line Vertical Maximum: up to 16,000,000 lines—for area scan sensors infinite line count—for linescan sensors
Pixel Clock Range	20 MHz to 85 MHz as follows: 8-bit: 8 taps @ 85 MHz, any tap configuration 10/12/14/16-bit: 4 taps @ 85 MHz, any tap configuration
Synchronization Minimums	Horizontal Sync minimum: 4 pixels Vertical Sync minimum: 1 line

Image Buffer	Available with 256 MB
Bandwidth to Host System	Approximately 1.5GMB/s.
Serial Port	Supports communication speeds from 9600 to 115 kbps
Controls	Compliant with Teledyne DALSA Trigger-to-Image Reliability framework Comprehensive event notifications Timing control logic for EXSYNC, PRIN and strobe signals Dual independent opto-coupled external trigger inputs programmable as active high or low (edge or level trigger, where pulse width minimum is 100ns) External trigger latency less than 1 µsec Supports multi-board / multi-camera synchronization Dual independent TTL Strobe outputs Quadrature (phase A & B) shaft encoder inputs for external web synchronization Opto-coupler input maximum frequency is 200 KHz RS-422 input maximum frequency is 5 MHz 4 opto-coupled general inputs (5V/24V) 4 opto-coupled general outputs I/O available on a CMD15 or DB37 connector
Processing *Dependant on user loaded firmware configuration*	**Output Lookup Table** one 8-bit in – 8-bit out one 10-bit in – 10-bit out one 12-bit in – 12-bit out three 8-bit in – 8-bit out (RGB) See "Output LUT Availability LUT Availability" on (page 71) for details. **Bayer Mosaic Filter**: Hardware Bayer Engine supports one 8, 10 or 12-bit Bayer camera input. Bayer output format supports 8 or 10-bit RGB/pixel. Zero host CPU utilization for Bayer conversion. **Flat Field Correction** (Shading Correction): Uses dedicated 256 MB memory bank. Real-time Flat-line and Flat-field correction. Compensates for sensor defects such as FPN, PRNU, defective pixels and variations between pixels due to the light refraction through a lens (Shading effect). PRNU (*Photo Response Non Uniformity*): PRNU is the variation in response between sensor pixels. FPN (*Fixed Pattern Noise*): FPN is the unwanted static variations in response for all pixels in the image.

Table 18: Board Specifications

Host System Requirements

X64 Xcelera-CL+ PX8 Dimensions

Approximately 6.5 in. (16.6 cm) wide by 4 in. (10 cm) high

General System Requirements for the X64 Xcelera-CL+ PX8

- PCI Express x8 slot compatible
- On some computers the X64 Xcelera-CL+ PX8 may function installed in a x16 slot. The computer documentation or direct testing is required.
- X64 Xcelera-CL+ PX8 operates correctly when installed in a multi-processor system (including Hyper-Threading multi-core processors).

Operating System Support

Windows XP, Windows Vista and Windows 7, either 32-bit or 64-bit

Environment

Ambient Temperature:	10° to 50° C (operation) 0° to 70° C (storage)
Relative Humidity:	5% to 90% non-condensing (operating) 0% to 95% (storage)

Table 19: Environment Specifications

Power Requirements

+3.3V:	1.1A (standby) 1.1A (during acquisition)
+12V:	1.0A (standby) 1.1A (during acquisition)

Table 20: Power Specifications

EMI Certifications

EC & FCC DECLARATION OF CONFORMITY

We : DALSA Montreal Inc.
7075 Place Robert-Joncas, Suite 142,
St. Laurent, Quebec, Canada H4M 2Z2

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 89/336 EEC on the approximation of the laws of member states relating to electromagnetic compatibility, as amended by directive 93/68/EEC:

FRAME GRABBER BOARD: Xcelera-CL + PX8

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

EN55022:1998- Residential, Commercial and Light Industry
EN61000-4-3: 1996 A1, 1998
EN61000-4-6: 2006
EN61000-4-2: 1995 A1: 1998 A2:2001
EN61000-4-4: 2004

Further declare under our sole legal responsibility that the product listed conforms to the code of federal regulations CFR 47 part 15 for a class A product.

St. Laurent, Canada — Location
2010/02/03 — Date

Eric Carey, ing
Director,
Research & Development

Figure 26: EMI Certifications

Connector and Switch Locations

X64 Xcelera-CL+ PX8 Board Layout Drawing

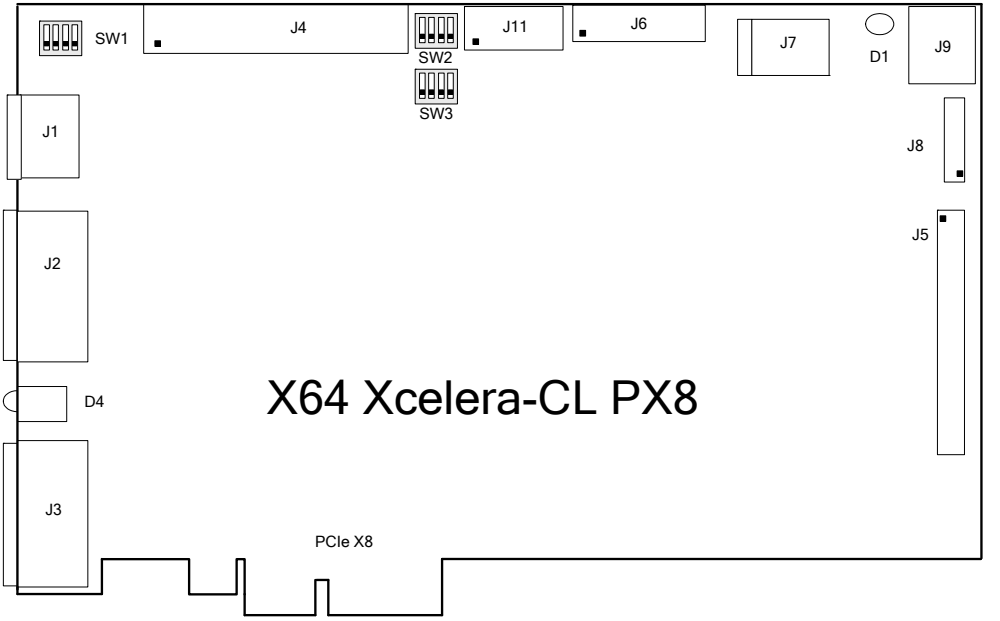

Figure 27: Board Layout

Connector, Switch, Jumper Description List

The following table lists components on the X64 Xcelera-CL+ PX8 board. Detailed information concerning the connectors or switches follows this summary table.

Location	Description	Location	Description
J1	External Signals connector CMD15	J11	Alternative RS-422 Shaft Encoder Input Connector
J2	Camera Link Connector (SDR)	J7	PC power to camera interface
J3	Camera Link Connector (SDR)		
J4	External Signals connector	D4	Camera/PCIe status LEDs
J9	Multi Board Sync	J5, J6, J8	Reserved
D1	Boot-up Status LED (refer to text)	SW1, SW2, SW3	Configuration micro-switches

Table 21: Board Connector List

Connector and Switch Specifications

X64 Xcelera-CL+ PX8 End Bracket Detail

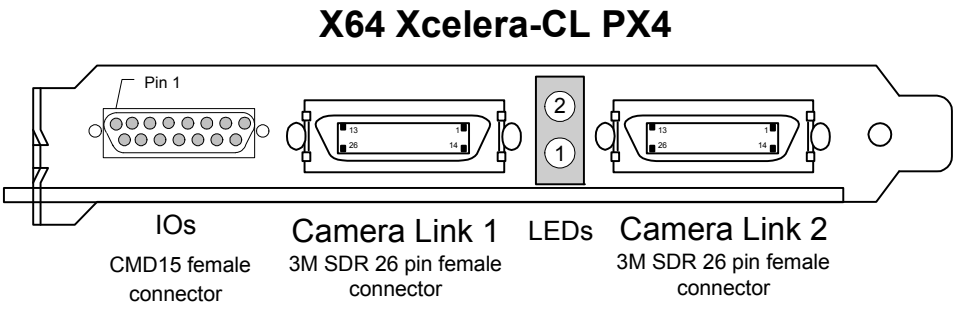

Figure 28: End Bracket Details

The hardware installation process is completed with the connection of a supported camera to the X64 Xcelera-CL+ PX8 board using Camera Link cables (see "Camera Link Cables" on page 121).

- The X64 Xcelera-CL+ PX8 board supports a camera with one or two Camera Link connectors (two Base or one Medium – see "Data Port Summary" on page 120 for information on Camera Link configurations).
- Connect the camera to the J2 connector with a Camera Link cable. When using a Medium or Full camera, connect the second camera connector to J3.

Note: If the camera is powered by the X64 Xcelera-CL+ PX8, refer to "External Signals Connector Bracket Assembly" on page 109 for power connections.

Contact Teledyne DALSA or browse our web site www.teledynedalsa.com/mv for information on X64 Xcelera-CL+ PX8 supported cameras.

Configuration Micro-switches

Three sets of 4 switches are used for user configurations not controlled by software. The following figure is a typical view of each switch set, shown with the individual switch set in the OFF position. Following the figure, each of the three switch sets is described. Refer to the board component layout for their positions.

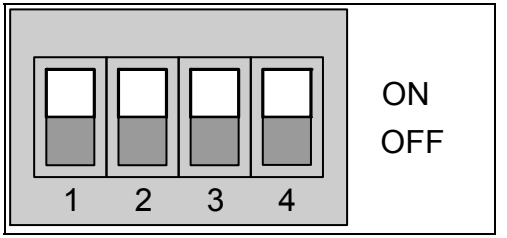

Figure 29: SW1, SW2, SW3 Component View

SW1: General Inputs Signal Switch Point

For each general input, select the threshold voltage detected as a logic high signal. See "Note 1: General Inputs Specifications" on page 104.

SW1 Switch Number	Assigned to	OFF Position	ON Position (default)
1	general input 1	Logic Transition at ~2 volts (preferred for differential signals)	Logic Transition at ~10 volts
2	general input 2		
3	general input 3		
4	general input 4		

Table 22: SW1 Switches

SW2: Normal/Safe Boot Mode & GEN2 Slot Workaround

The X64 Xcelera-CL+ PX8 powers up either in its normal state or a 'Safe Boot' mode required to load firmware under certain conditions. See the notes for SW2-1 following the table for details.

SW2 Switch Number	Assigned to	OFF Position (default)	ON Position
1	Boot Mode	Normal	Safe
2	GEN2 Slot Workaround	Disable (default)	Active
3	reserved		
4	reserved		

Table 23: SW2 Switches

SW2-1 Boot Mode Details

- **Normal Mode:** Board powers up in the normal operating mode.
- **Safe Mode:** With the computer off, move the switch to the ON position. This mode is required if any problems occurred while updating firmware. With the switch in the ON position, power on the computer and update the firmware again. When the update is complete, power off the computer, then move the switch to the OFF position. Power on the computer once again and update the Xcelera firmware. (See "Recovering from a Firmware Update Error" on page 36).

SW2-2 GEN2 Slot Workaround Details

- **Normal Mode:** Normal operation of the Xcelera-CL+ PX8
- **GEN2 Slot Workaround:** When using computers with GEN2 slots and the Intel 5400 chipset, there have been circumstances where the board is not detected. The Xcelera status LED 2 identifies this issue by continuously flashing red at boot time. In one example, with a Dell T5400 or T7400 computer, the computer displayed the following message BIOS:
  "Alert! Error initializing PCI Express slot".
  - Therefore, when using such a computer, with the Xcelera SW2-2 in the ON position, the computer should boot normally and the Xcelera should function. If this is not the case, please contact "Technical Support" on page 124 with details about your computer.

SW3: Trigger Inputs Signal Switch Point

For each trigger input, select the threshold voltage detected as a logic high signal. See "Note 3: External Trigger Input Specifications" on page 105.

SW3 Switch Number	Assigned to	OFF Position (default)	ON Position
1	trigger input 1	Logic Transition at ~2 volts (preferred for differential signals)	Logic Transition at ~10 volts
2	trigger input 2		
3	NA		
4	NA		

Table 24: SW3 Switches

Status LEDs Functional Description

D1 Boot-up status LED

Note: The LED D1 is mounted near the top edge of the board and is visible only with the computer cover off.

Color	State	Description
Red	Solid	FPGA firmware not loaded
Green	Solid	Normal FPGA firmware loaded
Blue	Solid	Safe FPGA firmware loaded
Green/Blue	Flashing	Test FPGA firmware loaded
Blue	Flashing	PCIe Training Issue – Board will not be detected by computer

Table 25: D1 Boot-up Status LED

Camera & PCIe status LED

Status LEDS are mounted between the camera link connectors—visible from the computer exterior.

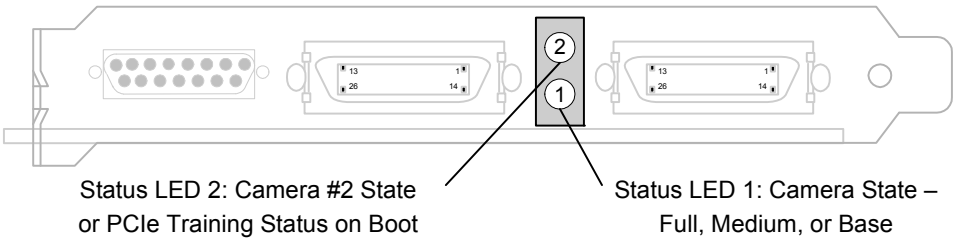

Figure 30: Status LEDs location

D4 - LED 1 Status

Color	State	Description
Red	Solid	No Camera #1 pixel clock detected
Green	Solid	Camera #1 pixel clock detected. No line valid detected.
Green	Slow Flashing ~2 Hz	Camera #1 pixel clock and line valid signal detected
Green	Fast Flashing ~16 Hz	Camera #1 acquisition in progress
Yellow	Solid	Safe Mode
Red/Green	Flashing	Test Mode

Table 26: LED 1 Status

D4 - LED 2 Status

Color	State	Description
Red	Solid	No Camera #2 pixel clock detected
Green	Solid	Camera #2 pixel clock detected. No line valid detected.
Green	Slow Flashing ~2 Hz	Camera #2 pixel clock and line valid signal detected
Green	Fast Flashing ~16 Hz	Camera #2 acquisition in progress
Yellow	Solid	Safe Mode
Red/Green	Flashing	Test Mode
Red	Flashing	PCIe Training Issue – Board is not be detected by computer.

Table 27: LED 2 Status

J2: Camera Link Connector 1

Name	Pin #	Type	Description
BASE_X0-	25	Input	Neg. Base Data 0
BASE_X0+	12	Input	Pos. Base Data 0
BASE_X1-	24	Input	Neg. Base Data 1
BASE_X1+	11	Input	Pos. Base Data 1
BASE_X2-	23	Input	Neg. Base Data 2
BASE_X2+	10	Input	Pos. Base Data 2
BASE_X3-	21	Input	Neg. Base Data 3
BASE_X3+	8	Input	Pos. Base Data 3
BASE_XCLK-	22	Input	Neg. Base Clock
BASE_XCLK+	9	Input	Pos. Base Clock
SERTC+	20	Output	Pos. Serial Data to Camera
SERTC-	7	Output	Neg. Serial Data to Camera
SERTFG-	19	Input	Neg. Serial Data to Frame Grabber
SERTFG+	6	Input	Pos. Serial Data to Frame Grabber
CC1-	18	Output	Neg. Camera Control 1
CC1+	5	Output	Pos. Camera Control 1
CC2+	17	Output	Pos. Camera Control 2
CC2-	4	Output	Neg. Camera Control 2
CC3-	16	Output	Neg. Camera Control 3
CC3+	3	Output	Pos. Camera Control 3
CC4+	15	Output	Pos. Camera Control 4
CC4-	2	Output	Neg. Camera Control 4
PoCL	1,26		+12 V (see note following this table)
GND	13, 14		Ground

Table 28: Camera Link Connector 1

Notes on PoCL support:

- Refer to Sapera's parameter CORACQ_PRM_POCL_ENABLE to enable PoCL and CORACQ_PRM_SIGNAL_STATUS/CORACQ_VAL_SIGNAL_POCL_ACTIVE to verify if the POCL is active. See also Sapera++ reference parameter SapAcquisition::SignalPoCLActive for the current state.
- PoCL state is maintained after a board reset

J3: Camera Link Connector 2

For X64 Xcelera-CL+ PX8 Full boards, Medium and Full Camera Link sources require cables connected to both J2 and J3.

For X64 Xcelera-CL+ PX8 Dual boards, J3 pinout is identical to J2.

Name	Pin #	Type	Description
MEDIUM _X0-	25	Input	Neg. Medium Data 0
MEDIUM _X0+	12	Input	Pos. Medium Data 0
MEDIUM _X1-	24	Input	Neg. Medium Data 1
MEDIUM _X1+	11	Input	Pos. Medium Data 1
MEDIUM _X2-	23	Input	Neg. Medium Data 2
MEDIUM _X2+	10	Input	Pos. Medium Data 2
MEDIUM _X3-	21	Input	Neg. Medium Data 3
MEDIUM _X3+	8	Input	Pos. Medium Data 3
MEDIUM _XCLK-	22	Input	Neg. Medium Clock
MEDIUM _XCLK+	9	Input	Pos. Medium Clock
TERM	20		Term Resistor
TERM	7		Term Resistor
FULL_X0-	19	Input	Neg. Full Data 0
FULL _X0+	6	Input	Pos. Full Data 0
FULL _X1-	18	Input	Neg. Full Data 1
FULL _X1+	5	Input	Pos. Full Data 1
FULL _X2-	17	Input	Neg. Full Data 2
FULL _X2+	4	Input	Pos. Full Data 2
FULL _X3-	15	Input	Neg. Full Data 3
FULL _X3+	2	Input	Pos. Full Data 3
FULL _XCLK-	16	Input	Neg. Full Clock
FULL _XCLK+	3	Input	Pos. Full Clock
GND	1, 13, 14, 26		Ground

Table 29: Camera Link Connector 2

Camera Link Camera Control Signal Overview

Four LVDS pairs are for general-purpose camera control, defined as camera inputs / frame grabber outputs by the Camera Link Base camera specification. These controls are on J2 and on J3 for the second Base camera input of the X64 Xcelera-CL+ PX8 in two Base configurations.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

Each camera manufacture is free to define the signals input on any one or all 4 control signals. These control signals are used either as camera control pulses or as a static logic state. Control signals not required by the camera are simply assigned as not used. Refer to your camera's user manual for information on what control signals are required.

Note 1: The X64 Xcelera-CL+ PX8 pulse controller has a minimum resolution of 100ns for line trigger signals, and resolution of 1µs for all other signal. When configuring the Camera Link control signals, uch as exposure control, etc. use values in increments of 1 µs.

Note 2: The internal line trigger frequency has a 1µs resolution.

The X64 Xcelera-CL+ PX8 can assign any camera control signal to the appropriate Camera Link control. The following screen shot shows the Sapera CamExpert dialog where Camera Link controls are assigned.

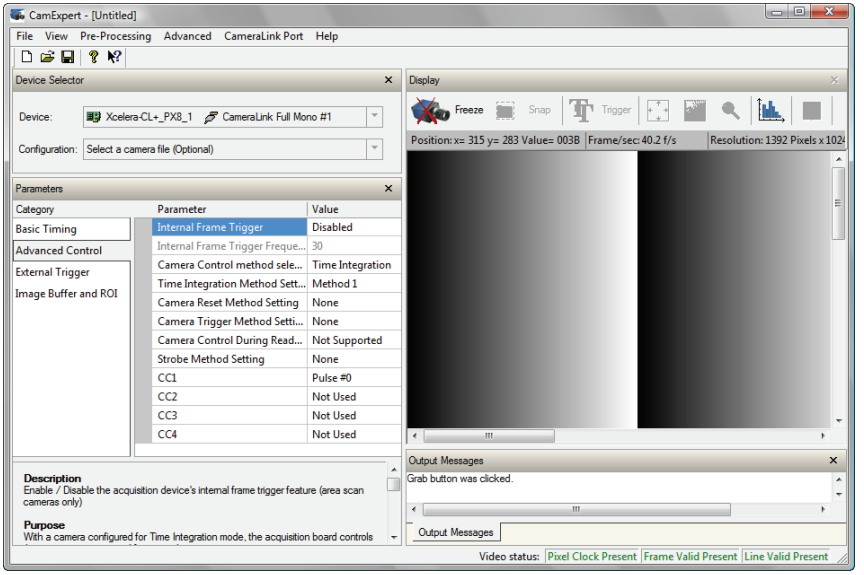

Figure 31: CamExpert - Camera Link Controls

Note that for Teledyne DALSA cameras such as the Falcon, where a CamExpert plug-in is available, these control signals will be pre-defined and hidden from view. A CamExpert plug-in will automatically configure required camera controls and only show user's parameters.

J4: External Signals Connector

J4 Pin Header Numbering Detail

2	4	...	38	40
1	3	...	37	39

Description	Pin #	Pin #	Description
Ground	1	2	Ground
General Input 1 + (all Opto-coupled — see note 1)	3	4	General Input 1 -
General Input 2 +	5	6	General Input 2 -
General Input 3 +	7	8	General Input 3 -
General Input 4 +	9	10	General Input 4 -
General Output 1 + (all Opto-coupled — see note 2)	11	12	General Output 1 -
General Output 2 +	13	14	General Output 2 -
General Output 3 +	15	16	General Output 3 -
General Output 4 +	17	18	General Output 4 -
External Trigger Input 1 + (all Opto-coupled — see note 3)	19	20	External Trigger Input 1 -
External Trigger Input 2 +	21	22	External Trigger Input 2 -
Opto-coupled Shaft Encoder Phase A + (see note 4)	23	24	Opto-coupled Shaft Encoder Phase A -
Opto-coupled Shaft Encoder Phase B +	25	26	Opto-coupled Shaft Encoder Phase B -
Ground	27	28	Strobe Output 1 (see note 5)
Ground	29	30	Strobe Output 2
Ground	31	32	Ground
Power Output 5 Volts, 1.5A max (see note 6)	33	34	Power Output 5 Volts, 1.5A max
Power Output 12 Volts, 1.5A max (see note 6)	35	36	Power Output 12 Volts, 1.5A max
Ground	37	38	Ground
Ground	39	40	Ground

Table 30: J4 Pin Header Pins Detail

J1 CMD15 Female External Signals Connector Descriptions

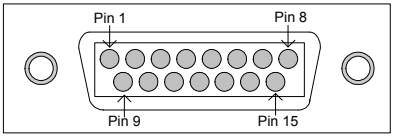

Figure 32: CMD15 Connector View

Description	Pin #	Pin #	Description
External Trigger Input 1 + (Opto-coupled — see note 3)	1	9	External Trigger Input 1 -
Opto-coupled Shaft Encoder Phase A + (see note 4)	2	10	Opto-coupled Shaft Encoder Phase A -
Opto-coupled Shaft Encoder Phase B +	3	11	Opto-coupled Shaft Encoder Phase B -
General Input 1 + (Opto-coupled — see note 1)	4	12	General Input 1 -
Ground	5	13	Strobe Output 1 (see note 5)
Ground	6	14	Power Output 5 Volts, 1.5A max (see note 6)
Ground	7	15	Power Output 12 Volts, 1.5A max (see note 6)
Ground	8		

Table 31: CMD15 Connector Detail

Blunt End Cable (OR-X8CC-IO15P) used with J1-CMD15

Wire Color	Pin #	Pin #	Wire Color
Black	1	9	Grey
Brown	2	10	White
Red	3	11	White/Black
Orange	4	12	White/Brown
Yellow	5	13	White/Red
Green	6	14	White/Orange
Blue	7	15	White/Yellow
Violet	8		

Table 32: CMD15 Cable No. OR-X8CC-IO15P Detail

Note 1: General Inputs Specifications

Each of the four General Inputs are opto-coupled and able to connect to differential signals (RS-422) or single ended source signals. These inputs generate individual interrupts and are read by the Sapera application. The following figure is typical for each Genera Input.

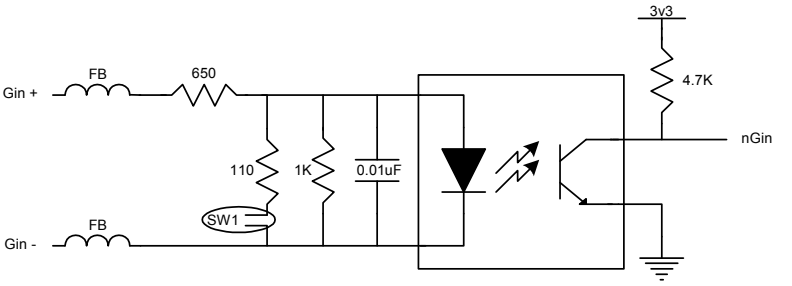

Figure 33: General Inputs Electrical Diagram

Input Details:

- For single ended signals, the Gin- pin is connected to ground. The switch point is ~10V by default and can be change to ~2V with **SW1**.
- Each input has a ferrite bead plus a 650-ohm series resistor on the opto-coupler anode.
- The 1K resistor and 0.01uF capacitor provide high frequency noise filtering.
- Maximum input voltage is 26V.
- Maximum input signal frequency is 25 KHz.
- Opto-coupler response time is 10µs for the rising edge signal.
- Opto-coupler response time is 27µs for the falling edge signal.

Note 2: General Outputs Specifications

Each of the four General Outputs are opto-coupled. Each output is an isolated open-collector NPN transistor switch. The following figure is typical for each General Output.

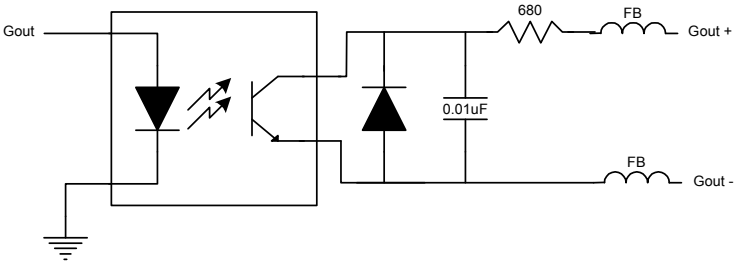

Figure 34: General Outputs Electrical Diagram

Output Details:

- Each output has ferrite beads plus a 680-ohm series resistor on the cathode (+) connection.
- The diode and capacitor provide reverse voltage protection and noise filter
- Maximum output device differential voltage is 25V.
- Maximum output device sink current is 35mA with 25V output differential.
- Maximum reverse voltage is 25V.
- Maximum output switching frequency is limited by driver and register access on the PCIe bus.

Note 3: External Trigger Input Specifications

The two Trigger Inputs are opto-coupled and compatible to differential signals (RS422) or single ended source signals. The following figure is typical for each External Trigger Input.

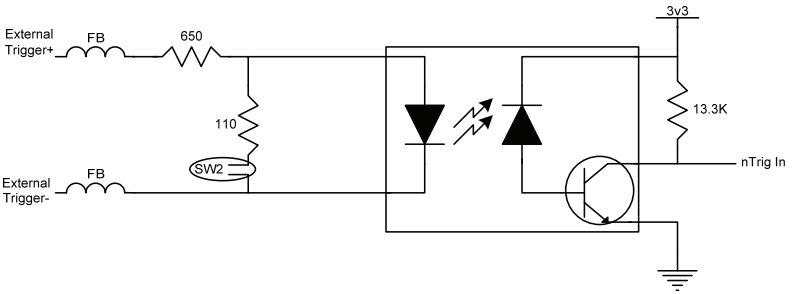

Figure 35: External Trigger Inputs Electrical Diagram

- For single ended signals, the External Trigger - pin is connected to ground. The switch point is ~2V by default to support TTL 5V signals and can be changed to switch at ~10V with **SW3** to support 24V industry standard signals.
- For RS422 differential signals, switch point must be selected to ~2V.
- Maximum external signal input voltage is 26V, irrelevant of the selected switch point.
- The incoming trigger pulse is "debounced" to ensure that no voltage glitch is detected as a valid trigger pulse. This debounce circuit time constant can be programmed from 1µs to 255µs. Any pulse smaller than the programmed value is blocked and therefore not seen by the acquisition circuitry. If no debouncing value is specified (value of 0µs), the minimum value of 1µs will be used.
- Each input has a ferrite bead plus a 650 ohm series resistor on the opto-coupler anode.
- Maximum input signal frequency is 100 KHz.
- Opto-coupler response time is 1.95µs for a rising signal.
- Opto-coupler response time is 2.9µs for a falling signal.
- Refer to Sapera parameters:
  CORACQ_PRM_EXT_TRIGGER_SOURCE
  CORACQ_PRM_EXT_TRIGGER_ENABLE

CORACQ_PRM_EXT_TRIGGER_LEVEL
CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL
CORACQ_PRM_EXT_TRIGGER_DETECTION
CORACQ_PRM_EXT_TRIGGER_DURATION

- See also *.cvi file entries:
  External Trigger Level, External Frame Trigger Level, External Trigger Enable, External Trigger Detection.
- External Trigger Input 2 used for two pulse external trigger with variable frame length line scan acquisition.

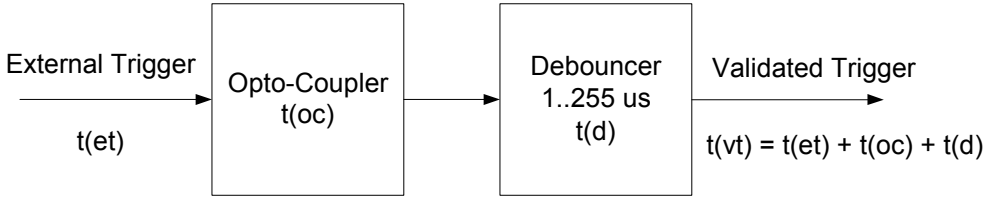

Figure 36: External Trigger Input Validation & Delay

Let	t(et) = time of external trigger in µs t(vt) = time of validated trigger in µs t(oc) = time opto-coupler takes to change state t(d) = debouncing duration from 1 to 255µs
trigger high	For an active high external trigger, t(oc) = 1.95µs: t(vt) = t(et) + 1.95µs + t(d)
trigger low	For an active low external trigger, t(oc) = 2.9µs: t(vt) = t(et) + 2.9µs + t(d)

Table 33: External Trigger Timing Specifications

Note: Teledyne DALSA recommends using an active high external trigger to minimize the time it takes for the opto-coupler to change state. Specifically, the opto-coupler response time is 1.95µs for active high compared to 2.9µs for active low.

If the duration of the external trigger is > t(oc) + t(d), then a valid acquisition trigger is detected. Therefore, the external pulse with active high polarity must be at least 2.95µs (if debounce time is set to 1) in order to be acknowledged. Any pulse larger than 3.9µs is always considered valid.

It is possible to emulate an external trigger using the software trigger which is generated by a function call from an application.

Note 4: Opto-Coupled Shaft Encoder Input Specifications

Dual Quadrature Shaft Encoder Inputs (phase A and phase B) are opto-coupled and able to connect to differential signals (RS-422) or single ended TTL 5V source signals. The following figure is typical for each input.

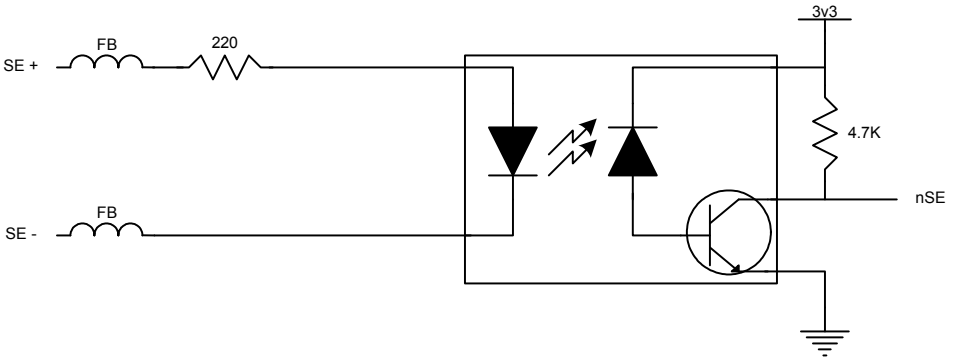

Figure 37: Opto-Coupled Shaft Encoder Input Electrical Diagram

- For single ended TTL 5V signals, the SE- pin is connected to ground. The switch point is ~2V.
- Maximum input voltage that can be applied is 6V.
- Each input has a ferrite bead plus a 220 ohm series resistor on the opto-coupler anode.
- Maximum input signal frequency is 200 kHz.
- Opto-coupler response time is 0.8µs for a rising signal.
- Opto-coupler response time is 1.7µs for a falling signal.
- See "Line Trigger Source Selection for Line scan Applications" on page 61 for more information.
- Refer to Sapera parameters:
  CORACQ_PRM_SHAFT_ENCODER_ENABLE CORACQ_PRM_SHAFT_ENCODER_DROP
  or refer to CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE
  CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION
  CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL (fixed at RS-422)
  CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE
  CORACQ_PRM_SHAFT_ENCODER_SOURCE
- See also *.cvi file entries:
  Shaft Encoder Enable, Shaft Encoder Pulse Drop, Shaft Encoder Source
  or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level, External Line Trigger Source.

Note 5: Strobe Output Specifications

Dual TTL Strobe outputs are provided. The following figure is typical for the strobe out.

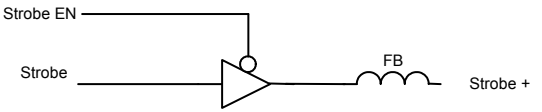

Figure 38: Strobe Output Electrical Diagram

- Each strobe output is a tri-state driver, enabled by software.
- Each strobe output is 5V TTL level.
- Each output has a ferrite bead.
- Maximum source current is 32mA typical.
- Maximum sink current is 32mA typical.
- Output switching is < 4.2ns typical.
- Refer to Sapera Strobe Methods parameters:
  CORACQ_PRM_STROBE_ENABLE
  CORACQ_PRM_STROBE_POLARITY
  CORACQ_PRM_STROBE_LEVEL
  CORACQ_PRM_STROBE_METHOD
  CORACQ_PRM_STROBE_DELAY
  CORACQ_PRM_STROBE_DURATION
- See also *.cvi file entries:
  Strobe Enable, Strobe Polarity, Strobe Level, Strobe Method, Strobe Delay, Strobe Duration.

Note 6: DC Power Details

- Connect the PC floppy drive power connector to J7 to supply DC power to the External Signal connectors. Both 5Vdc and 12Vdc are available on J1 or on the DB37 External Signals Bracket Assembly.
- Both the 5Volt and 12Volt power pins have a 1.5 amp re-settable fuse on the board. If the fuse trips open, turn off the host computer power. When the computer is powered again, the fuse is automatically reset.

External Signals Connector Bracket Assembly (Type 1)

The External Signals bracket (OC-X4CC-IOCAB) provides a simple way to bring out the signals from the External Signals Connector **J4 to a bracket mounted DB37**. Install the bracket assembly into an adjacent PC expansion slot and connect the free cable end to the board's J4 header. When connecting to J4, make sure that the cable pin 1 goes to J4 pin 1 (see the layout drawing "X64 Xcelera-CL+ PX8 Board Layout Drawing" on page 93).

External Signals Connector Bracket Assembly (Type 1) Drawing

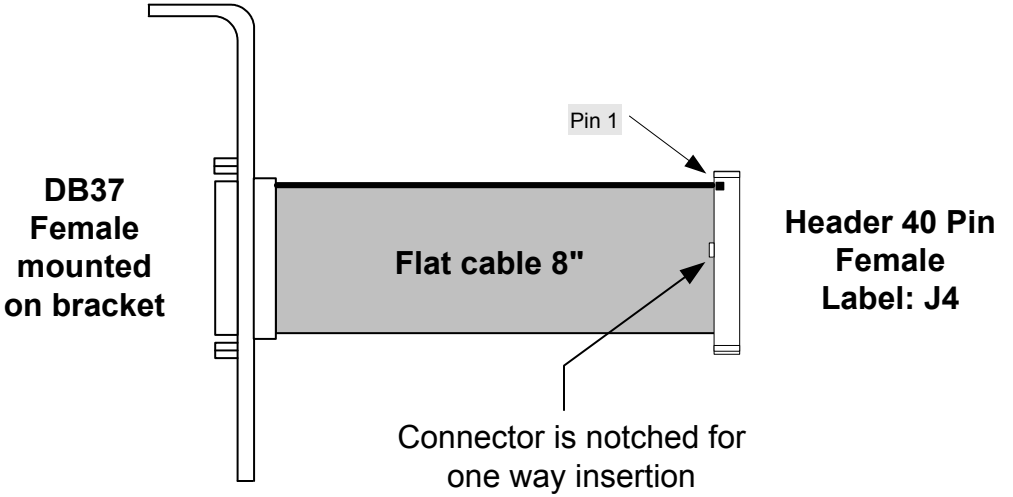

Figure 39: DB37 Output Cable

External Signals Connector Bracket Assembly (Type 1) Pinout

The following table defines the signal pinout on the DB37 connector. Refer to the table "J4: External Signals Connector " on page 102 for signal descriptions and notes.

DB37 Pin Number	Signal	J4 Connector Pin Number
1	Ground	1
20	Ground	2
2	General Input 1 +	3
21	General Input 1 -	4
3	General Input 2 +	5
22	General Input 2 -	6
4	General Input 3 +	7
23	General Input 3 -	8
5	General Input 4 +	9
24	General Input 4 -	10
6	General Output 1 +	11
25	General Output 1 -	12
7	General Output 2 +	13
26	General Output 2 -	14
8	General Output 3 +	15
27	General Output 3 -	16
9	General Output 4 +	17
28	General Output 4 -	18
10	External Trigger Input 1 +	19
29	External Trigger Input 1 -	20
11	External Trigger Input 2 +	21
30	External Trigger Input 2 -	22
12	Shaft Encoder Phase A +	23
31	Shaft Encoder Phase A -	24
13	Shaft Encoder Phase B +	25
32	Shaft Encoder Phase B -	26
14	Ground	27
33	Strobe Output 1	28
15	Ground	29
34	Strobe Output 2	30

16	Ground	31
35	Ground	32
17	+5V	33
36	+5V	34
18	+12V	35
37	+12V	36
19	Ground	37
—	—	38
—	—	39
—	—	40

Table 34: DB37 Cable Connector Details

External Signals Connector Bracket Assembly (Type 2)

The External Signals bracket (OR-X4CC-0TIO2) provides a simple way to bring out the signals from the External Signals Connector **J4 to a bracket mounted DB25**. External cables designed for the Teledyne DALSA X64-Xcelera-CL+ PX8 can connect directly.

Install the bracket assembly into an adjacent PC expansion slot and connect the free cable end to the board's J4 header. When connecting to J4, make sure that the cable pin 1 goes to J4 pin 1 (see the layout drawing "X64 Xcelera-CL+ PX8 Board Layout Drawing" on page 93).

External Signals Connector Bracket Assembly (Type 2) Drawing

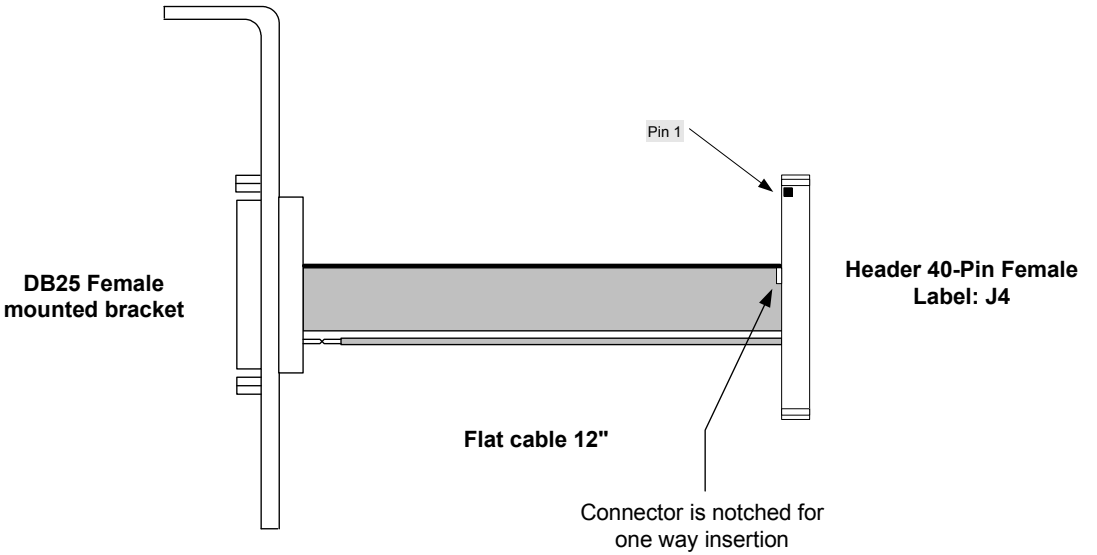

Figure 40: DB25 Output Cable

External Signals Connector Bracket Assembly (Type 2) Pinout

The following table defines the signal pinout on the DB25 connector.
Refer to the table "J4: External Signals Connector " on page 102 for signal descriptions.

DB25 Pin Number	Signal	J4 Connector Pin Number
6	External Trigger Input 1 +	19
19	External Trigger Input 1 -	20
7	External Trigger Input 2 +	21
20	External Trigger Input 2 -	22
8	Shaft Encoder Phase A +	23
21	Shaft Encoder Phase A -	24
9	Shaft Encoder Phase B +	25
22	Shaft Encoder Phase B -	26
11	Strobe Output 1	28
24	Ground	29
10	Strobe Output 2	30
14	Ground	31
15	Ground	38
16	Ground	39
25	Ground	40

Table 35: DB25 Cable Connector Details

J9: Multi-Board Sync

Interconnect multiple X64 Xcelera boards to synchronize acquisitions to one trigger or event. The trigger source can be either an external signal or internal software trigger. The board receiving the trigger is the Master board, while the boards receiving the control signal from the Master board are Slaves.

Setup of the master and slave boards is either by setting parameters via a Sapera application or by using CamExpert to configure two camera files (.ccf). For testing purposes, two instances of CamExpert can be run on the system with the frame grabbers installed.

Hardware Preparation

- Interconnect two, three, or four X64 Xcelera boards via their J9 connector. The 4 pin cable is wired one-to-one — i.e. no crossed wires. The cable must be as short as possible and the boards must be in the same system.

Sapera Application Programming

- **Master Board Software Setup:** Choose one X64 Xcelera as master. The Sapera parameter CORACQ_PRM_EXT_TRIGGER_SOURCE is set to either ***Mode 1–Output to Board Sync*** or ***Mode 2–Control pulse to Board Sync***. Other parameters are set as for any external trigger application, such as External Trigger enable, detection, and level. See Sapera documentation for more details.
- **Slave Board Software Setup:** The Sapera parameter CORACQ_PRM_EXT_TRIGGER_SOURCE is set to *From Board Sync*.

Sapera CamExpert Configuration

- **CamExpert Master Board Setup**:
  - Select the board to become the Master. From the CamExpert External Trigger parameter group, enable External Trigger and configure other parameters as required. Test the acquisition with the external trigger.
  - As shown in the CamExpert screen shot below, change the field for External Trigger Source to either ***Output to Board Sync*** or ***Control pulse to Board Sync***. See Sapera documentation for more details.

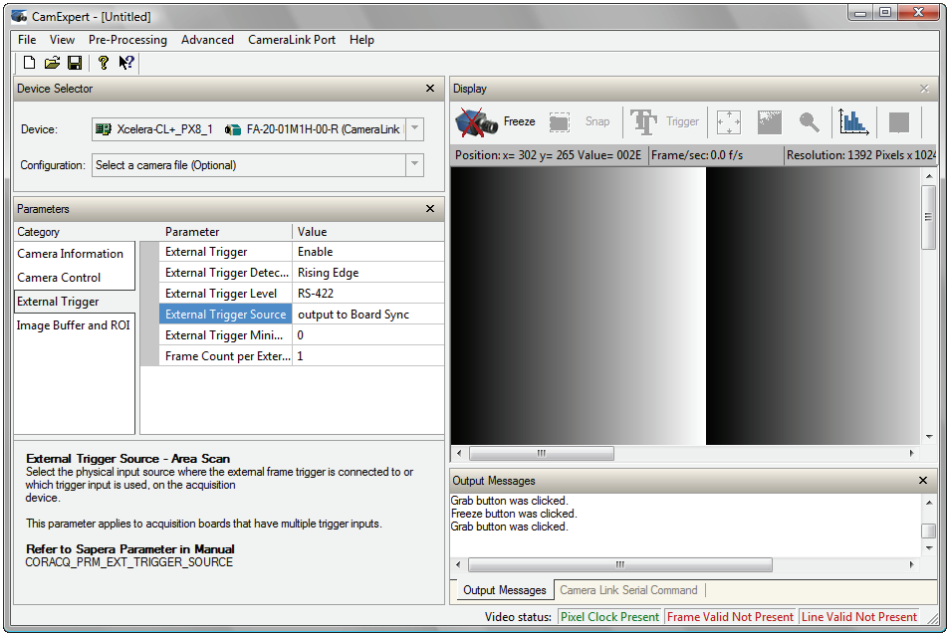

Figure 41: CamExpert – External Trigger Select

- **CamExpert Slave Board Setup:**
  - As shown in the CamExpert screen shot below, for any Slave board change the field for External Trigger Source to ***From Board Sync***. Other parameters are ignored, such as External Trigger detection and level.

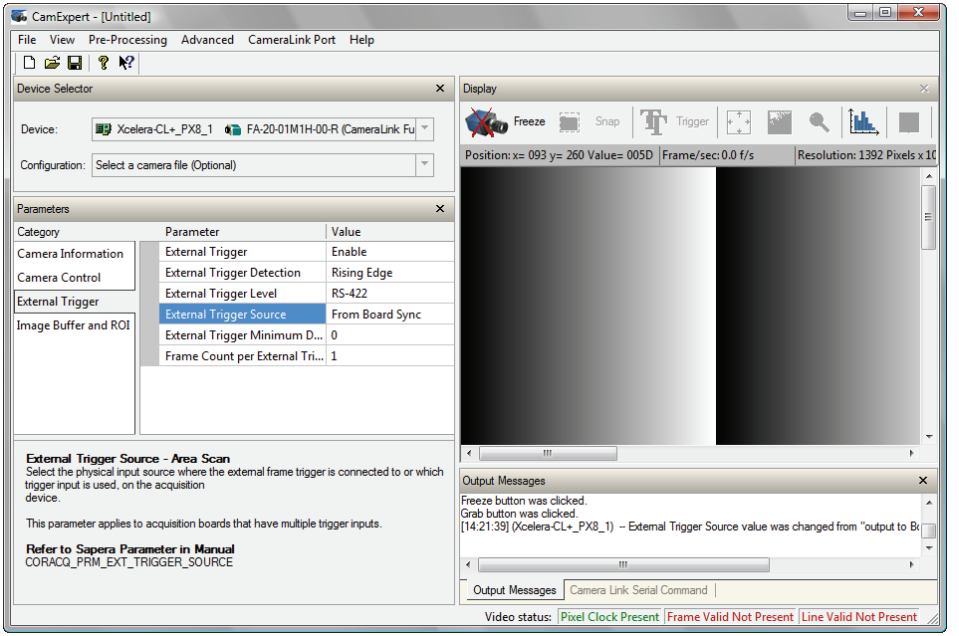

Figure 42: CamExpert – External Trigger Slave Board Setup

- **Test Setup:** The control application starts the acquisition on all slave boards. The acquisition process is now waiting for the control signal from the master board. Trigger master board acquisition and the acquisition start signal is sent to each slave board (with ~0.8µs delay max).

Contact Technical Support for additional information.

J11: RS-422 Shaft Encoder Input

J11 provides an alternative method to connect shaft encoder signals to the Xcelera-CL+ PX8 board, providing a higher maximum input signal frequency, but without the signal isolation provided by the opto-coupled shaft encoder inputs (on J1 or J4). The user or imaging application enables, via board parameters, which shaft encoder inputs are used for acquisition timing. For more information see "Line Trigger Source Selection for Line scan Applications" on page 61.

J11 Pin Header Numbering Detail

2	4	6	8	10
1	3	5	7	9

J11 Signal Descriptions

Description	Pin #	Pin #	Description
Ground	1	2	Ground
Shaft Encoder Phase A +	3	4	Shaft Encoder Phase A -
Ground	5	6	Ground
Shaft Encoder Phase B +	7	8	Shaft Encoder Phase B -
Ground	9	10	Ground

Table 36: J11-Connector Details

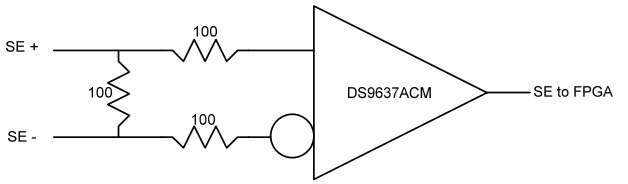

Figure 43: RS-422 Shaft Encoder Input Electrical Diagram

- For single ended TTL signals, connect a bias voltage to the RS-422 (-) input to ensure correct detection of the logic state of the TTL signal connected to the RS-422 (+) input. See the following section for connection methods.
- Maximum input voltage is 7V.
- All inputs have a 100-ohm series resistor.
- Maximum input signal frequency is **5 MHz.**
- Propagation Delay Time **Low to High** = 15ns Typical, 25ns Max.
- Propagation Delay Time **High to Low** = 13ns Typical, 25ns Max.
- See "Line Trigger Source Selection for Line scan Applications" on page 61 for more information.

- Refer to Sapera parameters:
  CORACQ_PRM_SHAFT_ENCODER_ENABLE CORACQ_PRM_SHAFT_ENCODER_DROP
  or refer to CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE
  CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION
  CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL (fixed at RS-422)
  CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE
  CORACQ_PRM_EXT_SHAFT_ENCODER_SOURCE
- See also *.cvi file entries:
  Shaft Encoder Enable, Shaft Encoder Pulse Drop, Shaft Encoder Source
  or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level, External Line Trigger Source.

TTL Shaft Encoder to RS-422 Input Block Diagram

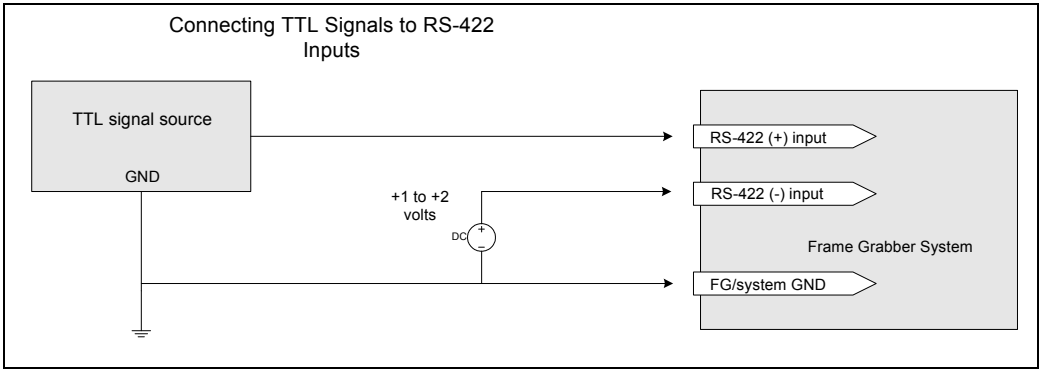

Figure 44: Connecting TTL to RS-422 Shaft Encoder Inputs

- RS-422 (-) input is biased to a DC voltage from +1 to +2 volts.
- This guarantees that the TTL signal connected to the RS-422 (+) input will be detected as a logic high or low relative to the (-) input.
- The TTL shaft encoder ground, the bias voltage ground, and the Xcelera-CL+ PX8 computer system ground must be connected together.

RS-422 (-) Input Bias Source Generation

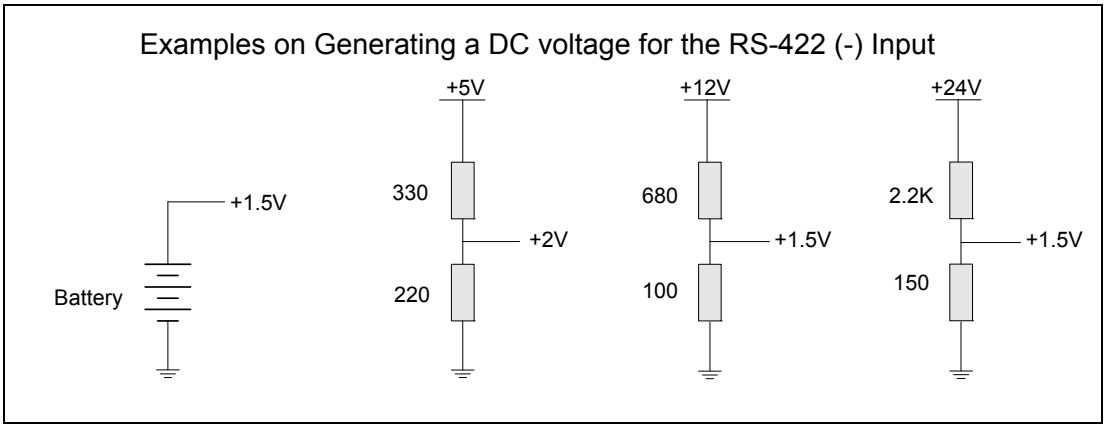

Figure 45: Generating a DC Bias Voltage

- DC voltage for the RS-422 (-) input can be generated by a resister voltage divider.
- Use a single battery cell if this is more suitable to your system.
- A DC voltage (either +5 or +12) is available on External Signals Connector J1 and J4.

Camera Link Interface

Camera Link Overview

Camera Link is a communication interface for vision applications developed as an extension of National Semiconductor's Channel Link technology. The advantages of the Camera Link interface are that it provides a standard digital camera connection specification, a standard data communication protocol, and simpler cabling between camera and frame grabber.

The Camera Link interface simplifies the usage of increasingly diverse cameras and high signal speeds without complex custom cabling. For additional information concerning Camera Link, see **http://en.wikipedia.org/wiki/Camera_Link**.

Rights and Trademarks

Note: The following text is extracted from the Camera Link Specification 1.1 (January 2004).

The Automated Imaging Association (AIA), as sponsor of the Camera Link committee, owns the U.S. trademark registration for the Camera Link logo as a certification mark for the mutual benefit of the industry. The AIA will issue a license to any company, member or non-member, to use the Camera Link logo with any products that the company will self-certify to be compliant with the Camera Link standard. Licensed users of the Camera Link logo will not be required to credit the AIA with ownership of the registered mark.

3M™ is a trademark of the 3M Company.

Channel Link™ is a trademark of National Semiconductor.

Flatlink™ is a trademark of Texas Instruments.

Panel Link™ is a trademark of Silicon Image.

Data Port Summary

The Camera Link interface has three configurations. A single Camera Link connection is limited to 28 bits requiring some cameras to have multiple connections or channels. The naming conventions for the three configurations are:

- Base: Single Channel Link interface, single cable connector
- Medium: Two Channel Link interface, two cable connectors
- Full: Three Channel Link interface, two cable connectors

A single Camera Link port is defined as having an 8-bit data word. The "Full" specification supports eight ports labeled as A to H.

Camera Signal Summary

Video Data

Four enable signals are defined as:

- FVAL Frame Valid (FVAL) is defined HIGH for valid lines
- LVAL Line Valid (LVAL) is defined HIGH for valid pixels
- DVAL Data Valid (DVAL) is defined HIGH when data is valid
- Spare A spare has been defined for future use

The camera provides the four enables on each Channel Link. All unused data bits must be set to a known value by the camera.

Camera Controls

Four LVDS pairs are reserved for general-purpose camera control, defined as camera inputs and frame grabber outputs.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

Note: the X64-Xcelera-CL+ PX8 by default implements the control lines as follows,
(using Teledyne DALSA Corporation terminology):

(CC1) EXYNC
(CC2) PRIN
(CC3) FORWARD
(CC4) HIGH

Communication

Two LVDS pairs are allocated for asynchronous serial communication to and from the camera and frame grabber. Cameras and frame grabbers should support at least 9600 baud.

- SerTFG Differential pair with serial communications to the frame grabber
- SerTC Differential pair with serial communications to the camera

The serial interface protocol is one start bit, one stop bit, no parity, and no handshaking.

Camera Link Cables

For additional information on Camera Link cables and their specifications, visit the following web sites:

3 M	http://www.3m.com/interconnects / *(enter Camera Link as the search keyword)*
Nortech Systems	http://www.nortechsys.com/intercon/CameraLinkMain.htm

Table 37: Camera Link Cables Suppliers

Contact Information

Sales Information

Visit our web site: www.teledynedalsa.com/mv

Email: mailto:info@teledynedalsa.com

Canada

Teledyne DALSA — Montreal office
7075 Place Robert-Joncas, Suite #142
St. Laurent, Quebec, Canada
H4M 2Z2

Tel: (514) 333-1301
Fax: (514) 333-1388

USA Sales

Teledyne DALSA — Billerica office
700 Technology Park Drive
Billerica, Ma.
01821

Tel: (978) 670-2000
Fax: (978) 670-2010

Asia Sales

Teledyne DALSA Asia Pacific
Ikebukuro East 13F
3-4-3 Higashi Ikebukuro,
Toshima-ku, Tokyo
Japan

Tel: +81 3 5960 6353
Fax: +81 3 5960 6354

European Sales

Teledyne DALSA Europe
Breslauer Str. 34
D-82194 Gröbenzell (Munich)
Germany

Tel: +49 - 8142 – 46770
Fax: +49 - 8142 - 467746

Technical Support

Submit any support question or request via our web site:

Technical support form via our web page: Support requests for imaging product installations, Support requests for imaging applications	http://www.teledynedalsa.com/mv/support
Camera support information	
Product literature and driver updates	

Glossary of Terms

Bandwidth
Describes the measure of data transfer capacity.

CAM
Sapera camera file that uses the file extension CCA by default. Files using the CCA extension, also called CAM files (CAMERA files), contain all parameters which describe the camera video signal characteristics and operation modes (i.e. what the camera outputs).

Channel
Camera data path that includes all parts of a video line.

Checksum
A value used to ensure data is stored without error. It is created by calculating the binary values in a block of data using some algorithm and storing the results with the data.

Contiguous memory
A block of physical memory, occupying consecutive addresses.

Firmware
Software such as a board driver that is stored in nonvolatile memory mounted on that board.

Frame buffer
An area of memory used to hold a frame of image data. A frame buffer may exist on the acquisition hardware or be allocated by the acquisition hardware device driver in host system memory.

Grab
Acquiring an image frame by means of a frame grabber.

Host
Refers to the computer system that supports the installed frame grabber.

Host buffer
Refers to a frame buffer allocated in the physical memory of the host computer system.

LSB
Least Significant Bit in a binary data word.

MSB

Most Significant Bit in a binary data word.

PCIe

Peripheral Component Interconnect Express. The PCIe bus is a high-performance expansion bus intended for interconnecting add-in boards, controllers, and processor/memory systems.

Pixel

Picture Element. The number of pixels describes the number of digital samples taken of the analog video signal. The number of pixels per video line by the number of active video lines describes the acquisition image resolution. The binary size of each pixel (i.e., 8-bits, 15-bits, 24-bits) defines the number of gray levels or colors possible for each pixel.

Scatter Gather

Host system memory allocated for frame buffers that is virtually contiguous but physically scattered throughout all available memory.

Tap

Data path from a camera that includes a part of or whole video line. When a camera tap outputs a partial video line, the multiple camera tap data must be constructed by combining the data in the correct order.

VIC

Sapera camera parameter definition file that uses the file extension CVI by default. Files using the CVI extension, also know as VIC files, contain all operating parameters related to the frame grabber board (i.e. what the frame grabber can actually do with camera controls or incoming video).

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